



Implementation of Digital Video Watermarking Scheme Based on FPGA

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Abstract— Objective of this scheme is to develop low power, robust and secure watermarking system for authentication of video. Here we present an FPGA based implementation of an invisible watermarking encoder. It consists of a watermark generator module and watermark insertion module. The system is initially simulated and tested for various attacks in MATLAB/ Simulink® and then prototyped on VERTEX-6 FPGA using VHDL. The watermarked video is same as that of original video with an average Peak-Signal-to-Noise Ratio (PSNR) of 46 dB.

Index Terms—Digital video watermarking, Discrete Wavelet Transform, Binary watermark.

I. INTRODUCTION

Due to increase in use of digital multimedia content large amount of data is transmitted using internet. Digital data can be modified and transfer easily. So there is need for copyright protection to prevent copying and distribution of digital data. Digital watermarking is technology which can be used for copyright protection of digital media [1]. Digital watermarking process consists of 2 steps. Watermark Embedding and detecting. The watermark encoder inserts watermark into the host video and the detector detects the presence of the watermark. Watermark key is used during the process of embedding and detecting the watermark. This watermark key is unique and private and known to only authorized parties. Applications of watermarking are copying prevention broadcast monitoring, authentication and data hiding [10].

Hien [2] has proposed a method for PCA transform to embed the watermark in each color channel of each frame. Same or multi-watermark can be embedded into the three color channels of the image in order to increase the robustness of the watermark. S.Bhargav Kumar [10] has combined the 4D-DWT technique for image segmentation and BPS for image compression to develop new technique which increased the robustness and invisibility of the watermarked image. Keshav S Rawat [13] presents digital watermarking methods for authorization against copying or piracy of color images.

Saraju P. Mohanty [11] has proposed an architecture and FPGA implementation of a spatial domain watermarking encoder. Mandeep Singh Saini [7] has implemented different digital image watermarking techniques in MATLAB SIMULINK for comparative analysis.

Watermark embedding in a video can be of two types frame based or stream based including AVI, MPEG-2 and MPEG-4 video frames/streams. In frame based embedding the watermark bits are embedded in the video by means of complete frame or tiles of the frame. In stream based watermark embedding technique, only the lines of the video frame are embedded. MPEG-4 has rapidly become one of the mainstream exchangeable video formats in the Internet today because it has high and flexible compression rate, low bit rate, and higher efficiency while providing superior visual quality.

This paper include following:

1. Design of Invisible robust video watermarking algorithms.
2. Design of MATLAB/Simulink® prototyping of the watermarking modules.
3. System Generator block is used to generate VHDL code.
4. VHDL based FPGA prototyping of the VLSI architectures which can be integrated in multimedia producing appliances.

Here we are using frame based watermarking technique. This system is implemented on Vertex-5 FPGA Board. MATLAB SIMULINK is used for software design and testing.

II. SCHEME OF IMPLEMENTATION

For implementation of robust video watermarking scheme following transforms are used.

1. Discrete Wavelet Transform (DWT)
2. Principle Component Analysis (PCA)

DWT is more efficient than other transform methods. A two level DWT decomposes image into low and high frequency components. Embedding the watermark in low frequencies obtained by wavelet decomposition increases the robustness with respect to various attacks. PCA is considered as a linear transform technique to convey most of information about the image to principal components. It is a technique of identify patterns in data, and expressing the data to emphasize their similarities and differences. It plots the data into a new coordinate system where the data with maximum covariance plotted together.

Here first video is divided into frames. Then luminance component of each frame is chosen and DWT is applied to it which results into different sub bands. These bands are again divided into different parts on which PCA is applied. For each part covariance matrix is calculated. Then each part is transform into PCA components. 32x32 bit watermark image is taken. This vector V is divided into four parts p1, p2, p3, and p4. Then each part is embedded into each of the corresponding sub bands. Inverse PCA is applied on the modified sub bands to obtain the modified wavelet sub-bands. By applying inverse DWT watermarked luminance component of the frames are obtained. Finally by reconstructing the watermarked frame watermarked video is obtained. This resultant video is interfaced with FPGA using Xilinx system generator.

A. Watermark embedding process

Step 1: Divide video into frames.

Step 2: Choose the luminance component Y of each frame and apply 2 levels DWT on it. This results in 16 sub bands.

Step 3: Divide each selected sub-bands with N/2xN/2 dimension into nxn non-overlapping parts where the number of parts is $k = (N/2xN/2) / (nxn)$.

Then, apply PCA to each part as describe bellow.

1. For each sub band S_i (nxn) compute mean of the part m_i , where S_i represent number of part i in the selected sub-band is. Then get zero mean A_i for each part as follows:

$$A_i = E(S_i - m_i) \tag{1}$$

2. For each part, calculate the covariance matrix C_i of the zero mean part A_i as

$$C_i = A_i * A_i^T \tag{2}$$

T symbol is used for matrix transpose operation.

3. Then each part is transform into PCA components by calculating the eigenvectors corresponding to Eigen values of the covariance matrix:

$$C_i \Phi = \lambda_i \Phi \tag{3}$$

Φ symbol is used for matrix of eigenvectors.

λ symbol is used for the matrix of Eigen values.

4. Compute the PCA transformation of each part to get uncorrelated coefficients by:

$$Y_i = \Phi^T A_i \tag{4}$$

Y_i symbol is used for principle component of the i^{th} part.

Step 4: Convert 32x32 into vector of zeros and ones.

$$V = \{v_1, v_2 \dots v_{32x32}\}$$

Step 5: Divide the vector V into n parts. Then each part is embedded into each of the corresponding LL and HH sub bands. The watermark bits are embedded with strength α into the maximum coefficient M_i of each PC block Y_i . The embedding equation is:

$$M_i = M_i' + \alpha W \tag{5}$$

α symbol is used to denote watermark embedding strength.

Step 6: Inverse PCA is applied on the modified PC block to obtain the modified wavelet block by using:

$$A_i = \Phi Y_i \tag{6}$$

Step 7: Apply the inverse DWT to obtain the watermarked luminance component of the frame. Finally reconstruct watermarked frame and obtain the watermarked video.

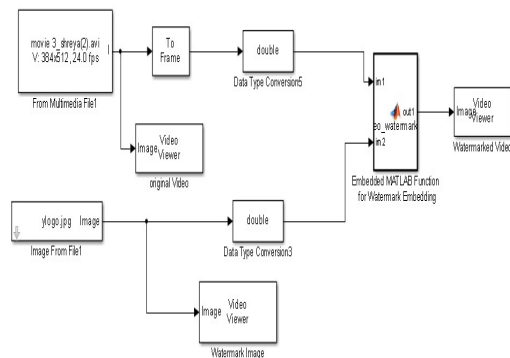


Fig.1. SIMULINK model for embedding system

B. Watermark extraction process

Step 1: Convert the watermarked video into frames. Each frame is converted to luminance representation.

Step 2: For each Y component, apply DWT to decompose Y into 16 multi-resolution sub bands. Choose LL and HH sub-bands and divide them into nxn non-overlapping parts.

Step 3: PCA transformation is applied on each part as described in the embedding procedure.

Step 4: Watermark is extracted by applying the following equation.

$$W = \frac{M_t^1 - M_t}{\alpha} \tag{7}$$

Step 5: Extracted watermark is compared with the original watermark by computing the similarity measure between them as follows:

$$NC = \frac{\sum_i \sum_j W(i,j).W'(i,j)}{\sum_i \sum_j W(i,j)^2} \quad (8)$$

Where, NC is the normalized correlation. NC value is 1 when the watermark and the extracted watermark are identical and zero if the two are different from each other. Software system design is done in MATLAB SIMULINK.

To measure performance of algorithm different attacks applied on video frame like noise addition, filtering, geometric attacks etc.

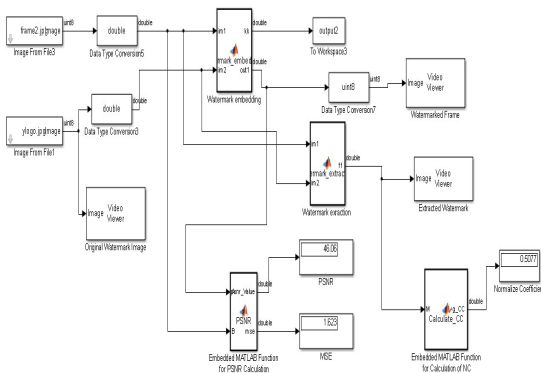


Fig 2. SIMULINK model for extraction system

III. FPGA BASED IMPLEMENTATION

Many DSP algorithms are designed using FPGAs instead of traditional ASICs or DSP processors. Xilinx has introduced new visual design methodology based on Matlab/Simulink interface. Xilinx had introduced its own Simulink tool which is called System Generator. This FPGA allows customizing the hardware logic in processor subsystem. It offers basic digital blocks with flexible interconnections to achieve high speed digital hardware realization. Here Matlab-Simulink and Xilinx software's are used along with Vertex-5 ML506 FPGA kit.

IV. RESULTS AND DISCUSSION

C. Matlab-Simulation Results

Fig. 3 shows video sequence 'movieview3_shreya.avi' of speed 24 frames / second and resolution 384*512. Using watermark image Fig.4 'ylogo.jpg' of size 32 × 32 is embedded with embedding strength $\alpha=0.5$. Using simulink model of watermark extraction original watermark is extracted from watermarked video frame.



Fig 3. Original Video movieview3_shreya.avi [384*512]



Fig.4 Watermark Image ylogo.jpg [32*32]

Results of embedding and extraction process are as shown in figures below figure 3 shows watermarked video frame having PSNR 46.06 db. Here watermarked frame appears exactly same as original video frame. And Fig 5.4 shows extracted watermark image having Normalize Coefficient of 0.5.







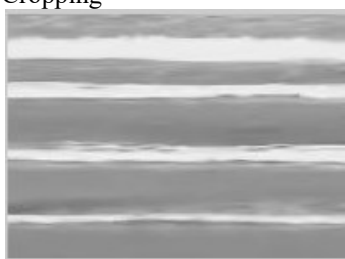

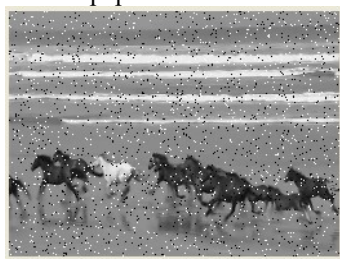
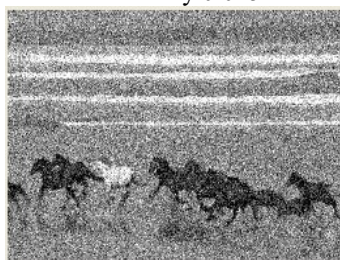
Fig.5 Watermarked Video frame [PSNR=46.06]



Fig.6 Extracted Watermark [NC=0.5]

B. Results of different Attacks

ATTACKS	PSNR (db)
Gamma correction by factor 1.1 	30.61
Contrast Adjustment by factor 10 	33.53

<p>Histogram Equalization</p> 	14.73
<p>Resizing</p> 	7.727
<p>Cropping</p> 	13.05
<p>Median Filtering</p> 	39.74
<p>salt and paper noise</p> 	18.61
<p>Gaussian noise by 0.025</p> 	16.3

System is prototyped using the Xilinx ML506 board containing a Virtex-5 Xc5v50t. Xilinx System Generator is used to generate VHDL code. Very High Speed Integrated Circuit Hardware Description Language (VHDL) is used to program FPGA. Actual output of watermarked video frame is displayed on monitor screen through VGA port.

C. Results of Synthesis Process

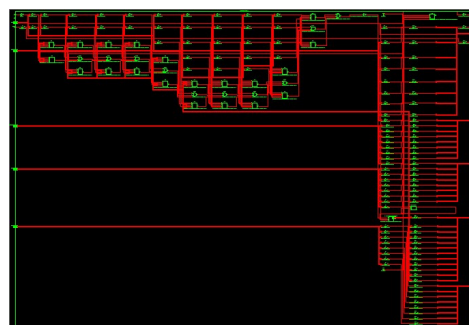


Fig.8 Hierarchical RTL schematic of watermarking process



Fig.7 Output of watermarking system on Monitor

Bit stream of the system is downloaded from PC side with USB J-Tag cable on Virtex 5 ML 506 board with the device xc5v50t. The output of the system is displayed on VGA monitor as shows above.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1	28800	0%
Number of Slice LUTs	21	28800	0%
Number of fully used LUTs-FF pairs	0	22	0%
Number of bonded IOBs	113	480	23%
Number of BUFG/BUFGC TRLs	1	32	3%

Table 2. Device utilization summaries

Logic and memory utilization of our system is shown in table 2. It shows the amount of resources required is relatively small. Number of registers Used is 1 out of 28800, no. of input output blocks used are 113 out of 480 i.e. only 23 % are get used.

Timing report summary: Minimum input arrival time before clock: 0.506 ns Maximum output required time after clock: 2.861 ns.

V. CONCLUSIONS

By observing the simulation results it shows that watermarking algorithm can work successfully for grayscale video sequence. After application of different attacks quality of watermarked video frame is unchanged so system is imperceptible and robust against common video processing attacks. Advantage of watermarking system is that we can embed the watermark in LL band without high degradation. As simulink is used VHDL code is automatically generated. Hardware implementation of this algorithm is performed on Virtex 5 (ML-506) FPGA. Device utilization summary shows that amount of resources required are relatively small. This watermarking based authentication provides a solution for fingerprinting and copy right protection and real time authentication.

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