



A Wideband Variable-Gain Amplifier for High Frequency Applications

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Abstract— The design of a fixed gain amplifier is useful when the input signal is of the same strength, but if the signal strength varies, it becomes difficult to amplify it to a level such that it can be utilized by the blocks present further in the communication link. A variable gain amplifier (VGA) can be used to provide a variable gain for input signals of varying strength. Hence VGAs have become an necessary blocks in wireless transmitter-receiver sections. VGAs are present as the second or third block in the wireless receiver section. The ability of VGA to amplify signals of varying strength increases the dynamic range of the receiver. A novel basic cell design has been presented, which can be cascaded in order to achieve more gain for the overall VGA. The basic cell of VGA has a relatively constant bandwidth from 3.5 to 4 GHz for the desired frequency range. The current consumption of the basic cell is only a few milli-amperes from a 1.2V supply. The robustness of the unit cell is verified by means of ADS simulation.

Keywords— basic cell, variable gain amplifier (VGA), CMOS, linear gain, low power.

I. INTRODUCTION

Amplifier design, conventionally comprises of designing an amplifier which provides a fixed gain to the input signal, where the output signal is an amplified version of the input signal. The design of a fixed gain amplifier is useful when the input signal is of the same strength, but if the signal strength varies, it becomes difficult to amplify it to a level such that it can be utilized by the blocks present further in the communication link. A variable gain amplifier (VGA) can be used to provide a variable gain for input signals of varying strength. Hence VGAs have become an necessary blocks in wireless transmitter-receiver sections. VGAs are present as the second or third block in the wireless receiver section. The ability of VGA to amplify signals of varying strength increases the dynamic range of the receiver.

High gain must be provided for input signals with low strength and low gain is needed for the input signal with high strength. The gain of a VGA can be varied or controlled by a control voltage, hence it is also called as voltage-controlled amplifier. As the control voltage varies, the gain of the amplifier also varies, but this change in gain must be linear i.e., the gain of the

amplifier should gradually increase or decrease with change in control voltage. The voltage-controlled amplifier can be further divided into two types depending on the type of control voltage applied. If the control voltage is analog, then it is called as a variable gain amplifier, whereas if it is digital in nature, it is called as programmable variable gain amplifier (PGA).

The PGAs, with digital control voltage, implements variable gain using resistors and capacitors as switches. The drawbacks of this method is that it leads to signal phase distortion and in order to increase the number of steps in the gain of amplifier, control bits need to be increased. The presence of capacitors in controlling the gain increases the time between application of control voltage and changes in the gain. For many applications, discrete shifts in gain is not preferred, the shifts in gain must be rather even. This can be easily achieved by an analog controlled VGA. The analog controlled VGAs are usually implemented by varying the transconductance of the load stage with respect to the input stage.

Just as the gain should linearly vary with respect to control voltage, the gain should also remain constant for the entire frequency range. The gain must be constant and ripple free with minimum variations. Therefore, a linearly varying gain with respect to control voltage and a constant gain with respect to the entire frequency range are two important desirable characteristics of a VGA.

Besides accurate gain characteristics, the power consumption of VGA should be minimum, hence CMOS technology has been preferred. Previously VGAs have been implemented using Silicon-Germanium technology but it is not intended for low power and low cost applications. CMOS is preferred in areas which require low power and minimal cost. To keep the power consumption minimum, the supply voltage chosen must be less, this in turn limits the gain of the amplifier. If the supply voltage is less, the current consumption is less, getting high gain from such low current consuming devices is all likely impossible if proper linear gain characteristics are required.

In short, the impetus of VGA design is better linear gain accuracy, more bandwidth and minimal power consumption. Other than that, smaller size, higher yield and better robustness are always the driving force in practice.

II. LITERATURE REVIEW

The location of the VGA in wireless communication is as shown in Fig. 1. The LPF will first filter the signal and then feed it to the VGA block for amplification. Mostly coarse gain tuning is provided by PGAs in RF front end and then fine gain tuning is provided by analog controlled VGAs. The dual scheme can be reduced to just analog controlled VGA if the design is robust and the dynamic range is more.

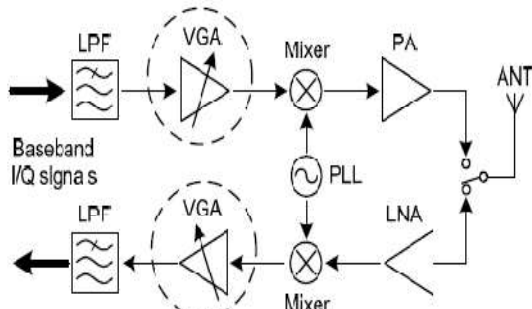


Fig. 1. A simple RF system showing the location of VGA[2]

To understand the design and working of a VGA, the following parameters must be considered.

A. Variation in gain

Variation in gain is the difference between the maximum and minimum gain that the VGA can provide within the desired frequency range. The variation in gain must be small and it should be such as to cover the entire frequency range. This can either be realized by a single stage VGA or by connecting many stages in cascade.

B. Error in gain

The deviation in gain from an ideal straight line is called as error in gain. the error in gain must be minimum if better linear gain characteristics are required.

C. Bandwidth

The frequency where the gain power falls to 70% with respect to flat gain is called as bandwidth. The definition is trivial for a single frequency response. In some places the gain peaks and falls, the bandwidth hence can also be defined as -3dB with respect to gain at low frequency or at peak gain. the aim is always to keep the gain almost flat for the entire bandwidth.

D. Relation between linear gain and noise

Low noise and highly linear gain are desired characteristics of VGA. The relation between noise, linear gain and sensitivity is important. Sensitivity is the smallest gain that the VGA can amplify. The more is the

noise, the less is the sensitivity and less linear gain. Low noise and linear gain are always sought after but there exists a trade-off between them.

E. Power

For low power applications, the power consumption of a VGA is an important parameter. It should be low so that there is less heat dissipation and extended life in case of battery operated devices. The less the supply voltage, noise and linear gain degrades which hampers the overall performance of the system.

F. S parameters

They differ from any of the two port network parameters, in a manner that S-parameters do not use open or short circuit conditions to characterise the system, instead, matched loads are used. These parameters applicable for all frequencies but are mostly used for circuits operating at radio frequency (RF) where signal power and energy considerations are easily determined than currents and voltages. S-parameters are frequency dependent, so frequency must be mentioned for any

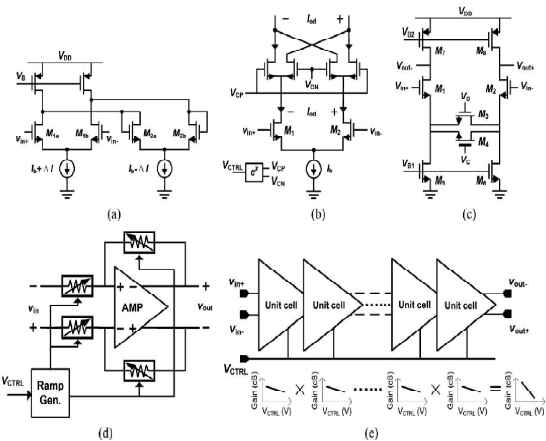


Fig. 2. State-of-the-art VGA topologies[2]

S-parameter measurement.

There exists an exponential relation between control voltage and gain. This can be given by Taylor's series as,

$$e^{2x} \approx \frac{1+x}{1-x} \quad (1)$$

The expansion of this series cannot directly be implemented because of increase in design complexity. Hence approximations which simplify the design challenge are made:

$$e^{2x} \approx \frac{k+(1+ax)^2}{k+(1-ax)^2} \quad (2)$$

where k can be taken as 12, this is given in more detail in [4].

Due to low supply voltage and limited gain of active devices, desired gain cannot be given by a single device. A remedy is to connect many such devices in cascade.

This increases the overall gain. The Taylor's series can now be approximated as:

$$e^{-x} \approx \left(1 + \frac{x}{n}\right)^n \quad (3)$$

where n is the number of stages in cascade.

Fig 2 gives a brief idea about the existing state of the art VGA topologies. Fig 2 (a) shows the topology of VGA, which can be implemented by varying the transconductances of the load stage with respect to the input stage. Fig 2 (b) and (c) show VGA of similar type but the load stages have been modified to establish a more better exponential relation between the applied control voltage and resultant linear gain variation. Fig 2 (d) depicts the implementation of VGA using ramp based technique. This topology is implemented by adding ramp signals to achieve a flat gain. Ramp signals are then added or subtracted to vary the gain. This topology makes use of variable resistors for the implementation of variable gain and hence is not preferred, since it will take up more chip area for implementation. A proper linear can be implemented is shown by this topology.

As previously discussed, due low supply voltage the gain provided by only a single stage is not sufficient to meet the requirements. If amplifiers are cascaded as shown in Fig 2 (e), the gain of each stage is added to get the targeted gain. The gain bandwidth product is always a constant. Hence increased gain can be achieved at the cost of reduced bandwidth. Hence there arises a need to design a basic block of VGA which will have a large bandwidth and suitable gain to fulfil the design requirements when connected in cascade. This block is termed as a "cell". Many such cells can be cascaded to implement the overall VGA to meet the gain and bandwidth requirements.

The design of the basic cell must be complete and robust in itself because every error in the basic cell will get multiplied when all the cells are connected in cascade. If 10 cells are to be connected in cascade such that the overall error in gain of the VGA system must be less than 1 dB, then the error in gain of each basic cell needs to be less than 0.1 dB. The gain of the basic cell must vary linearly for the gain of the overall system to vary accurately. When the basic cells are connected in cascade, the current consumption of the overall increases, hence the overall power consumption of the circuit also increases. Hence the basic unit cell design must be robust and meet all the requirements to fulfil the specifications.

III. DESIGN OF BASIC CELL

The schematic of basic cell is as shown in Fig. 3. The MOSFETs, M_1 and M_2 are input differential pair of transistors. Input is provided at the gates of transistors M_1 and M_2 . M_3 sets the overall current conditions of the circuit, hence it is the current source of the circuit. The current source can be implemented by a current mirror. For implementation of linear gain, NMOS transistors M_4 and M_5 , which act as load, are biased below threshold

region. The control voltage is applied at the gates of transistors M_4 and M_5 . MOSFETs M_6 and M_7 are also load transistors but are biased in the saturation region.

The gain of the basic cell is given by:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1,2}}{g_{m4,5} + g_{m6,7}} \quad (4)$$

where g_m is the trans-conductance of the respective MOSFET. As the control voltage is applied at transistors M_4 and M_5 , the current changes through the load. This is rewritten as equation (5):

$$A_V = \frac{g_{m1,2}}{g_{m4,5} + g_{m6,7} + \Delta g_{m4,5} + \Delta g_{m6,7}} \quad (5)$$

The bias conditions of input differential pair transistors M_1 and M_2 are kept constant, thus the current relationship between $I_{DS,4,5}$ and $I_{DS,6,7}$ can be expressed as:

$$I_{DS,1,2} = I_{DS,4,5} + I_{DS,6,7} \quad (6)$$

and thus,

$$\Delta I_{DS,4,5} = -\Delta I_{DS,6,7} \quad (7)$$

As the NMOS load MOSFETs M_4 and M_5 are biased below threshold region, the trans-conductance $g_{m,4,5}$ is expressed as:

$$g_{m,4,5} = \frac{2I_{DS,4,5}}{nV_T} \quad (8)$$

Whereas, the other NMOS load MOSFETs M_6 and M_7 are biased in saturation region, and the trans-conductance $g_{m,6,7}$ can be expressed as:

$$g_{m,6,7} = \sqrt{2\mu_P C_{ox} \left(\frac{W}{L}\right)_{6,7} \cdot \sqrt{I_{DS,6,7}}} \quad (9)$$

Differentiating $g_{m,4,5}$ with regard to $I_{DS,4,5}$ and $g_{m,6,7}$ with regard to $I_{DS,6,7}$,

$$\Delta g_{m,4,5} = \frac{2}{nV_T} \Delta I_{DS,4,5} \quad (10)$$

$$\Delta g_{m,6,7} = \frac{2\mu_P C_{ox} \left(\frac{W}{L}\right)_{6,7}}{g_{m,6,7}} \Delta I_{DS,6,7} \quad (11)$$

Substituting (7), (10), and (11) into (5) leads to

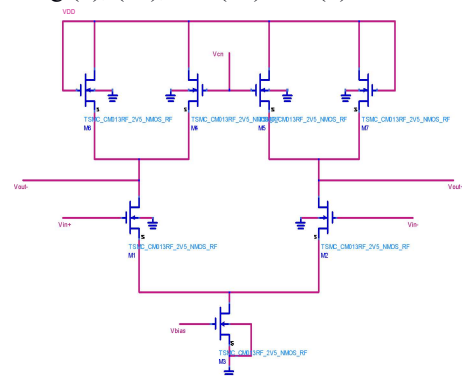


Fig. 3. Schematic of the Unit Cell

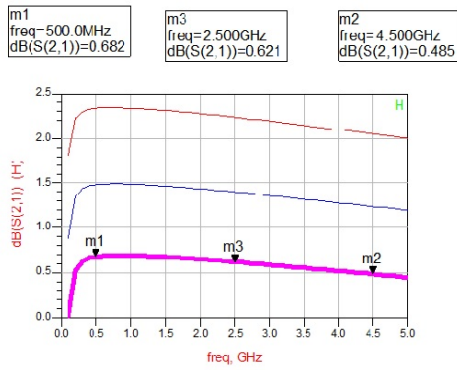


Fig. 4. Gain vs. Frequency response of the unit cell

$$A_V = \frac{g_{m,1,2}}{g_{m,4,5} + g_{m,6,7} + \left(\frac{2}{nV_T} - \frac{2\mu_p C_{ox}}{g_{m,6,7}} \left(\frac{W}{L} \right)_{6,7} \right) \Delta I_{DS,4,5}} \quad (12)$$

As M_4 and M_5 are biased below threshold region, the current $I_{DS,4,5}$ can be expressed as

$$I_{DS,4,5} = I_{O,4,5} \left(\frac{W}{L} \right)_{4,5} \exp \left(\frac{kV_{G,4,5} - V_{S,4,5}}{nV_T} \right) \quad (13)$$

where $I_{O,4,5}$ is the below threshold gate leakage current. k is to be taken as 0.7 for the entire region below threshold. Differentiating $I_{DS,4,5}$ with regard to $V_{G,4,5}$ gives the expression of $I_{DS,4,5}$ as:

$$\Delta I_{DS,4,5} = \frac{k}{nV_T} I_{O,4,5} \left(\frac{W}{L} \right)_{4,5} \times \exp \left(\frac{kV_{G,4,5} - V_{S,4,5}}{nV_T} \right) \Delta V_{G,4,5} \quad (14)$$

The W/L ratios of all the MOSFETs needs to be chosen so that all the devices operate in their proper regions of operation. The width of all the MOSFETs must be kept minimum to check the current flowing through them but decreases the overall gain of the circuit.

For MOSFETs M_1 and M_2 , the more the width, gain is more but gain falls rapidly, The less the width, more flat is the gain

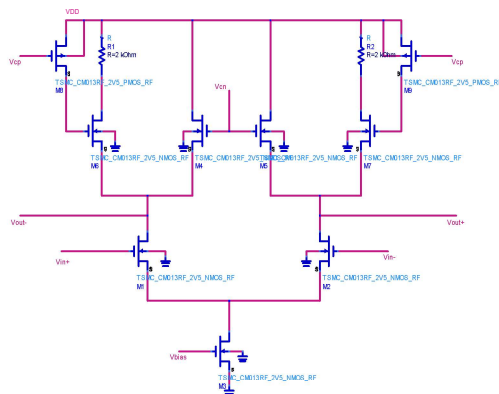


Fig. 5. Schematic of unit cell with extended bandwidth

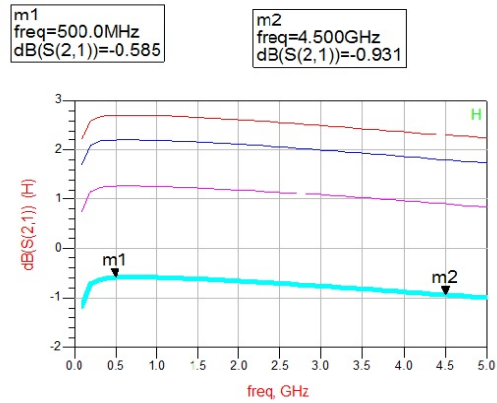


Fig 6. Gain vs. Frequency response of the unit cell with extended bandwidth

but the gain is less. For M_3 , increase in width leads to increase in overall current consumption of the basic cell circuit, hence it provides bias conditions for the circuit. For M_4, M_5, M_6, M_7 , more the width, the overall gain increases, but gain begins to fall rapidly with respect to increase in frequency i.e., flat gain response is lost. Whereas less the width, the overall gain decreases, though the response is flat.

IV. DESIGN OF BASIC CELL WITH BANDWIDTH EXTENSION

The bandwidth of the basic cell can be extended by modifying the load stage as shown in Fig. 4. PMOS transistors are introduced in the load stage, these along with the load resistor R_L are used to control the ripples present in the flat gain response. Their connection is as shown in Fig. 4. To minimize the design complexity of the unit cell as well as effectively control the gain peaking, a control-voltage generator is designed and is presented. In this way, V_{CP} can be generated, and dynamically follows the variation of V_{CN} so that the peaking can be effectively controlled [1]. The impedance looking into the source of M_6, M_7, Z_L can be expressed as:

$$Z_L = \frac{1 + sC_{GS}R_G}{g'_{m,6,7} + sC_{GS}} \quad (15)$$

Substituting this as $1/g_{m,6,7}$ in (4) gives:

$$A_V = \frac{g_{m,1,2}(1 + sC_{GS}R_G)}{g'_{m,6,7} + sC_{GS} + g_{m,4,5}(1 + sC_{GS}R_G)} \quad (16)$$

A zero is now in the denominator of (16), due to the existence of gate resistor, R_G . The corner angular frequency of the zero is $\omega_z = -1 / C_{GS}R_G$.

By observation, the dominant pole of the output node, $\omega_{p,out}$ is expressed as:

$$\omega_{p,out} = - \frac{g_{m,4,5} + g_{m,6,7}}{C_{total,out}} \quad (17)$$

where $C_{\text{total, out}}$ is the overall total capacitance of output node.

Equations (15)–(17) show how the gate-peaking technique can be used for bandwidth extension of the basic cell.

MOSFETs M_8 and M_9 are operated in the linear region of operation. The device widths of MOSFETs M_8 and M_9 must also be properly selected for them to effectively control the gain. The less the width, more gain peaking occurs. The more the width, the gain peaking reduces making the gain flat. The less is the load resistance R_L , more is the current consumption of the overall circuit whereas increase in the resistance value decreases the current consumption but the design process becomes extremely complicated.

TABLE ERROR! NO SEQUENCE SPECIFIED. : OBTAINED RESULTS FROM SIMULATIONS IN ADS 2009

| Sr. No. | Parameters | Obtained Values |
|---------|--------------------|-----------------|
| 1 | Gain (dB) | ~2.7 |
| 2 | Bandwidth (GHz) | ~4 to 4.5 |
| 3 | Error (dB) | ± 0.3 |
| 4 | Supply Voltage (V) | 1.2 |
| 5 | Current (mA) | 5.87 |
| 6 | Technology (nm) | 130 |

In practice, an ideal flat gain response is not possible to achieve, but by setting proper widths of devices as mentioned above, ripple can be reduced from the gain. more is the ripple in the gain, more are the chances of it adversely affecting the bandwidth, which in turn adversely affects the linear gain performance. Hence there always is a trade off between ripple in gain and bandwidth.

V. PERFORMANCE SUMMARY

To verify the performance of the unit cell, simulations have been performed in advanced design system (ADS) 2009 using 130-nm CMOS technology. The basic unit cell with extended bandwidth has a almost constant gain for around 4 GHz. Maximum bandwidth achievable by a single basic cell is 2.7 dB from a 1.2 V supply. The control voltage needs to be varied from 0.6V to 1V to achieve a linear gain. The gain variation is less than 0.35 dB for 4 GHz bandwidth. Moreover the basic cell only consumes 5.87 mA of current. These basic cells can be connected in cascade to obtain more gain.

VI. CONCLUSIONS

The design of an analog controlled VGA using a novel technique which breaks up the overall VGA into basic cells is presented. To justify the tradeoff between gain and bandwidth, a system-level analysis for the gain and bandwidth requirements of the basic cell is given. Based on the analysis, a simple, yet robust basic cell is presented. The basic cell adopts a unique gain control method, which can accurately adjust the gain of the VGA without compromising any other performance. To

verify the concept, the simulation of the VGA is done on a standard 130-nm CMOS technology. The measured result show that the frequency range over which the gain remains almost flat is more than 4 GHz, while the power consumed is minimum from a 1.2-V supply. Moreover, a linear gain range of 2.7 dB with only 0.3-dB gain error is achieved. The presented basic block can be used to build a VGA which can be used in applications which require less power consumption and more bandwidth.

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