



# Sub-threshold Design using SCL for Low Power Applications

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**Abstract** –Sub-threshold circuits have gained a lot of importance due to advent of ultra-low power consumption. Power dissipation and delay plays an important role in achieving optimized performance. This paper primarily focuses on Sub-Threshold Source Coupled Logic (STSCl) for building digital circuits and systems at very low voltages with optimum performance and desirable energy savings. The performance characteristics of inverter and the basic gates are operating in the sub-threshold region have been analyzed in 90nm technology. These gates are further used to implement digital systems which would work at low supply voltages and consume less power. Simulation results show the advantages of STSCl over CMOS based logic.

**Index Terms**– CMOS, SCL, STSCl, Sub-CMOS, Ultra low power

## I. INTRODUCTION

In digital design, a lot of attention has been given to the design of high performance microprocessors. However, in recent years, the demand for power sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as personal digital assistants, cellular phones, medical applications, wireless receivers, and other portable communication devices [1], [2].

In context of these applications, digital computation using sub-threshold leakage current has gained a wide interest to achieve ultra-low power consumptions in portable computing devices. Both logic and memory circuits have been extensively studied with design consideration at various levels of abstraction. It can be concluded that using sub-threshold operation, significant power savings can be achieved in circuits using low to medium operating frequencies [1], [2].

This paper is organized as follows. The scope of sub-threshold design study is presented in Section II. Section III provides an insight into Source Coupled Logic (SCL) and its operation in sub-threshold region. In Section IV, experimental results of inverters and basic gates along with further implementation into nine stage ring

oscillator and 16 bit multiplier are presented. Finally, conclusions are drawn in Section V.

## II. SUBTHRESHOLD OPERATION

### A. Sub-threshold Region

Sub-threshold conduction refers to the current that flows between source and drain of the MOS transistor when the transistor operates in the weak inversion region. This occurs when the gate-to-source voltage,  $V_{gs}$  is below the threshold voltage,  $V_t$  of the MOS transistor given by  $V_{gs} < V_t$ . The devices work in this region and employ leakage currents to charge and discharge load capacitances. Here, the source to drain weak inversion current is the main leakage contributor, while other leakage currents such as gate tunneling current and gate induced drain leakage current are typically considered negligible. The sub-threshold current of an MOS transistor is very sensitive to temperature and process variations, which causes fluctuations in the threshold voltage of the transistor and have an exponential effect on the sub-threshold current. Equation 1 gives a simple model for the sub-threshold drain current.

$$I_{ds} = I_{dso} \cdot \exp\left(\frac{(V_{gs} - V_{th})}{n} \cdot V_t\right) \left(1 - \exp(-V_{ds}/V_t)\right) \quad (1)$$

where,  $I_{dso}$  is the drain current when  $V_{gs} = V_t$ . This equation provides an insight about how small changes in the voltages exponentially changes the drain current. Figure 1 illustrates the region of operation of digital sub-threshold circuits.

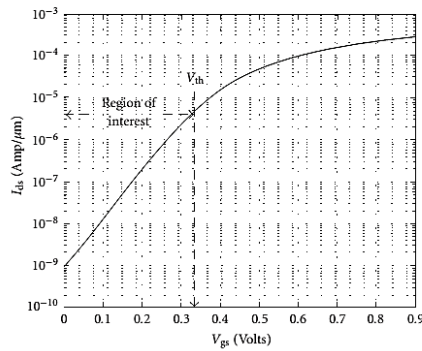


Fig. 1. Region of operation of digital sub-threshold logic [1].

### B. Critical Design Challenges of Sub-threshold Circuits

This section illustrates an interesting insight into the challenges faced while working with energy-constrained applications whilst taking advantage of sub-threshold circuits.

(1) Redesigning the devices can be beneficial to the sub-threshold circuits. For increased performance, device optimization is important for sub-threshold circuits in addition to technology scaling. Process, Voltage, and Temperature (PVT) are more pronounced in sub-threshold circuits and there is need to come up with a novel method to combat this variability [1], [2].

(2) Though static CMOS is functional in sub-threshold region, it is of not much use because of short channel effects. Other logic families which are resilient to such effects must be pursued [1], [2].

(3) In sub-threshold circuits, the supply voltage is much less than the threshold,  $V_{dd} < V_t$ . This attributes to an exponential increase in delays as the voltage scales, thereby increasing the leakage energy. Alternate avenues must be exploited to overcome this drawback [1], [2].

(4) Device scaling offers a reduction in gate capacitance and for super threshold circuits, it reduces switching energy and gate delay. However, for sub-threshold circuits, the case might not be the same because of exponential dependencies on  $V_{dd}$ ,  $V_t$  and inverse sub-threshold slope. So, improved scaling strategies must be introduced to tackle scaling in sub-threshold circuits [1], [2].

## III. CONCEPT OF SOURCE COUPLED LOGIC (SCL)

This section briefly illustrates an overview of SCL theory, topology and its behavior under sub-threshold regime.

### A. SCL – Overview and Topology

Source coupled logic, also known under the more general term current mode logic (CML) is a group of logical families that use transistor differential pairs to

switch a constant bias current towards one of two branches representing the two terminals of a differential output signal. In a MOS implementation, an NMOS tail transistor biased with a constant gate voltage acts as a current source that draws a constant current from the supply. Logic operation takes place by steering the tail current to one of the two load devices. This can be achieved by network of differential pairs controlled by the (differential) gate input voltages. The output signal is created by two ‘resistors’ that convert the difference in current in their respective branches into a differential output voltage.

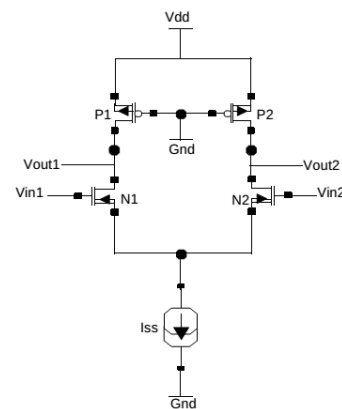


Fig. 2. Schematic of SCL inverter.

A basic SCL inverter circuit diagram can be seen in Fig. 2 which is differential in nature. The immediate choice over differential logic is due to its noise immunity respect to switching. Even though wiring differential logic is a complex task and also implementing it in the CMOS logic, put a barrier in scaling the supply voltage to a minimum level, which in current nanometer electronic platforms is a drawback. When input voltage for the NMOS N1 tops that of NMOS N2, the output voltage,  $V_{out2}$ , at that point starts to lower down and attains a steady state. During this time  $V_{out1}$  gets charged up to the supply voltage level via PMOS P1. The output swing,  $V_{SW}$  achieved can be defined by the following,

$$V_{SW} = V_{out1} - V_{out2} = 2 \cdot R_d \cdot I_{ss} = 2 \cdot V_{del} \quad (2)$$

where  $I_{ss}$  is the bias current,  $R_d$  is the equivalent load resistance for the PMOS devices, and  $V_{del}$  is the voltage drop across the PMOS P2. This provides an additional advantage of using differential logic by having an output swing two times the actual drop across the load. The optimal performance in such a topology can be achieved, with the total current flowing through the circuit being equal to  $I_{ss}$  and having a smaller load resistance for a smaller delay.

### B. Sub-threshold SCL (STSCCL)

In Sub-Threshold SCL (STSCCL) circuits, the load is a PMOS transistor where the bulk terminal is connected to the drain (Fig. 3). This device is biased in Weak

Inversion (WI) and provides a large equivalent resistance.

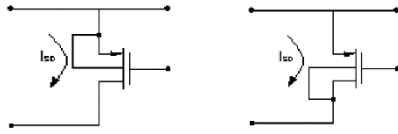


Fig. 3. Conventional (left) and the STSCL load device (right).

The PMOS load device that has been used for further studying the behavior of STSCL gates and its operation under sub threshold region. The PMOS load is mainly implemented by connecting the bulk of a PMOS to its drain causing a formation of reverse-biased diode; Figure 3.4 shows a cross-section view of the reverse biased diode formation between drain and the substrate of the PMOS giving a high resistance value. This high resistive value helps the SCL logic to operate at sub-threshold region at a very small applied bias current.

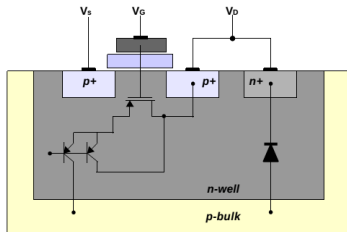


Fig. 4. Cross section of PMOS load device showing the parasitic components.

The equation for the equivalent resistance of the this new PMOS load is given by,

$$R_{dnew} = \left( \frac{\frac{n_p \cdot V_T}{I_{SD}}}{(n_p - 1) \exp(V_{SD}/V_T) + 1} (\exp(V_{SD}/V_T) - 1) \right) \quad (3)$$

where,

$$V_{SD} = \frac{V_{SD}}{n_p V_T} \quad (4)$$

and

$$I_b = I_0 \cdot \exp\left(\frac{V_{SG} - V_{T0}}{n_p V_T}\right) \quad (5)$$

From the Eqn. 3, the  $R_{dnew}$  can be controlled by the source to drain current flow which for an STSCL circuit is equivalent to the bias current. Also from the equation, the resistance is exponentially dependent on the source to gate voltage allowing further tune-ability of the resistive value over a large range. The tuning of the resistive value feature allow the STSCL gate to be operated at different region and conditions without modifying much of the devices internal parameters like size, etc.

The logic evaluation in STSCL circuits can be performed correctly if the swing voltage is larger than about  $4nV_T$  where  $n$  is the sub threshold slope factor (varies with the operating temperature and process) for NMOS devices and  $V_T$  the thermal voltage.

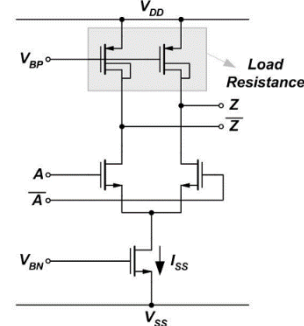


Fig. 5. Schematic of STSCL inverter.

One more crucial thing that comes into consideration during the performance analysis, is the operation time or speed for the SCL gate running at sub-threshold or linear region.

$$t_d = \frac{V_{swing} \cdot C_{load}}{I_{bias}} \quad (3)$$

where the delay for the sub-threshold SCL is inversely proportional to bias current. The trade-off in this case is that more  $I_{bias}$  means more power consumption

The most important parameter for an STSCL gate to run properly and consume less power is to control the amount of  $I_{bias}$  flowing through the logic. Theoretically for the STSCL,  $I_{bias}$  can be reduced to a value closes to the sub-threshold leakage through the circuit. As mentioned above a voltage swing equivalents to  $4nV_T$  is enough to drive an STSCL gate in sub-threshold region, but for maintaining controlled operation over that region requires a stable and controlled biasing. This is achieved by using a biasing circuit that will keep the swing at the output under check and on a desired value. An example of simple bias circuit used for the STSCL inverter gate is shown in Fig. 6.

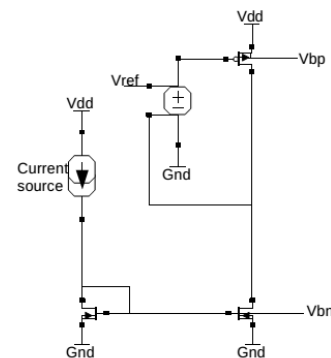


Fig. 6. Simple bias circuit for STSCL gates.

The bias circuit in Fig.6 should be attached with the STSCL gates for proper operation. The current mirror section of the bias circuit must function properly. Otherwise, if there is any small deviation on the generated bias current from the bias circuit, it will counter with a large deviation across the PMOS load devices, hence this circuit is more sensitive towards mismatch due to process deviations. It is important, prior to designing the bias circuit, that the NMOS devices in the bias circuits has to be taken of higher threshold and they should contribute low leakage, otherwise the output swing will deviate considerably and the power consumption might also increase. To redeem this problem the amplifier's gain can be tuned in such a way, that a swing higher than  $4nV_T$  can be achieved, without disrupting the required performance.

#### IV. CIRCUIT IMPLEMENTATION AND RESULTS

In this section, performance analysis and comparison of CMOS and STSCL gates is illustrated.

##### A. Circuit Implementation

In this section, the focus will be on different gates implemented using STSCL. These logic gates are further used in digital sub systems such as 9-stage ring oscillator and a 16-bit multiplier. The following have been simulated in Cadence Virtuoso in 90 nm technology.

For the ring oscillator, the oscillation frequency range was observed as well as the corresponding power dissipation to find the circuit limitations and the output response for the ring oscillator at 0.5 V supply

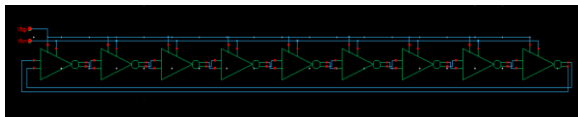


Fig. 7. Schematic of 9 stage ring oscillator using STSCL logic.

For 16-bit multiplier, conventional architectures are used and no power optimization techniques, for example pipelining or voltage scaling per se, are applied to any of the systems. The supply voltage used for the CMOS logic is  $V_{dd} = 0.5V$  and for the STSCL it is  $V_{dd} = 0.2V$ . The CMOS logic did not operate correctly at supply voltages below  $V_{dd} = 0.4V$ .

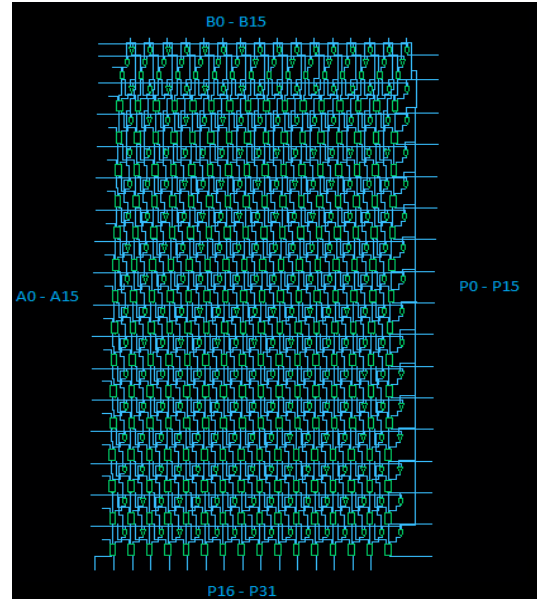


Fig. 8. Schematic of 16-bit Array Multiplier using STSCL logic.

##### B. Experimental Results

In this section, the power and delay calculations of the STSCL and CMOS based logic gates (inverter and Basic gates) are tabulated in Table 1

TABLE I

INVERTER			
Logic	Power (nW)	Delay ( $\mu s$ )	PDP (pW-s)
CMOS	1.022	1.16	1.185
STSCL	0.52	0.69	0.359
AND/NAND GATE			
Logic	Power (nW)	Delay ( $\mu s$ )	PDP (pW-s)
CMOS	1.054	1.35	1.423
STSCL	0.65	0.78	0.507
OR/NOR GATE			
Logic	Power (nW)	Delay ( $\mu s$ )	PDP (pW-s)
CMOS	1.057	1.35	1.427
STSCL	0.655	0.81	0.531
XOR/XNOR GATE			
Logic	Power (nW)	Delay ( $\mu s$ )	PDP (pW-s)
CMOS	1.126	2.061	2.321
STSCL	0.73	1.31	0.956
D FLIP FLOP			
Logic	Power (nW)	Delay ( $\mu s$ )	PDP (pW-s)
CMOS	2.315	2.28	5.278
STSCL	1.905	1.56	2.972

Fig. 9. Analysis of Power Consumption and Delay for CMOS and STSCL gates at  $V_{dd} = 0.2V$ 

TABLE II

Logic	Supply (Volts)	Output Frequency (GHz)	Power Consumption ( $\mu W$ )
CMOS	0.4	0.382	0.921
	0.5	0.784	2.67
STSCL	0.4	0.279	0.519
	0.5	0.536	1.72

Fig. 10. Analysis of Power Consumption and Delay for CMOS and STSCL ring oscillator at  $V_{dd} = 0.4V$  and  $0.5V$ 

The simulation results go in coherence with the basic concept of a ring oscillator where the frequency of oscillation increases with increasing the supply voltage. Even though power consumption is lower for the STSCL a difference is found in the output frequency, so to a certain extent this comparison is not viable. This is however not a matter of high concern from an application perspective, as it is less likely that the STSCL will be used for any application with operating frequency ranging above Megahertz and more likely to be used in applications related to low power issues.

TABLE III

Logic	Power (mW)	Delay ( $\mu s$ )	PDP(nW-s)
CMOS	0.849	58.47	49.641
STSCL	0.593	79.33	47.042

Fig. 10. Analysis of Power Consumption and Delay for CMOS and STSCL based 16-bit array multiplier

The area (in turn, the delay) of the STSCL multiplier is considerably higher than that of CMOS because many number of transistors are used to treat differential logic (and bias circuits), but it must be remembered that the STSCL logic is being run at a very low supply voltage compared to CMOS.

## V. CONCLUSION

Sub-threshold region operation plays a very important role in order to reach a very low power-energy consumption specification. This type of specification would be used in implementation of an e.g. modern-day distributed sensor networks. Designers, nowadays, apply power reduction techniques in every level of abstraction in order to achieve optimum level of power reduction. This paper deals with power-energy reduction methods at the circuit-level abstraction. The results obtained for the STSCL based circuits show that there is indeed an average reduction of 25–30 % in energy consumption over CMOS-based counterparts, without much

degradation in performance. However, the area overhead is slightly higher in STSCL because of the presence of differential logic and replica bias circuit.

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