Analytical Modeling of Surface Potential for Cylindrical Gate-All-Around in as Nanowire FET

[1]Jitendra Prasad, [2]Amit Agarwal, [3]P.C.Pradhan, [4]B.P. Swain

[1,2,3]Dept. of Electronics and Communication Engineering, SMIT, Sikkim, India
[4]Centre for Material Science and Nanotechnology ,SMIT, India

Abstract: In this paper, we are going to study the potential distribution of the Cylindrical Gate All Around (CGAA) MOSFETs by solving the 2-D Poisson's equation in the cylindrical coordinate system.The effects of the device parameters like the drain bias voltage(V_{DS} ranging from -0.5 to 0.5V), oxide thickness(t_{ox} ranging from 1nm to10nm),temperature(ranging from 100K to 700K),gate source voltage(V_{GS} ranging from -1 to 1V)for the channel length of 25nm are studied and their effect on the surface potential are observed. The device is modeled using Matlab Code.

Index Terms: MOSFETs, CGAA FET, Short Channel Effects (SCEs),Surface Potential.

I. INTRODUCTION

The aggressive scaling of CMOS technology has been the attention of electronic industry in the last few decades[6]. The main advantage for scaling is the necessity of achieving higher packing density, improvingthe performance of SOI chips, and cost effective electronic devices.[2] However, the scaling of the CMOS transistor comes on the cost of raising several effects such as Drain Induced Barrier Lowering, Hot Carrier Effects etc known as short channel effects (SCEs)[3].

The phenomenon of short channel effects in MOSFET has been known since the late 1970s.As gate length are reduced, threshold voltage are seen to decrease and leakage currents are seen to increase[1].This is a consequence of fact that as gate lengths are reduced, the depletion regions associated with the source to body and drain to body regions become closer to each other, since depletion regions are region of high electric field, they facilitate carrier transport directly between the source and drain regions[3].These short channel effects, have a large impact on the performance of the device as it degrades the performance. To overcome these problem the gate length should be atleast six times greater then the natural length of a device. This natural length gives the extension of the electric field from the source and drain in the channel[4].

An excellent way to increase the gate control over the channel is to have an extra gate. This extra gate would help improve the immunity of the channel. Also multigate transistors provide high speed, low power configuration, higher noise tolerance[10].

In this model we are using InAs nanowires compared to others such as InP because InAs nanowires has the electron mobilities of 6000cm^{2}V^{-1}s^{-1} which is high compared to InP therefore it is used in high mobility applications such as in MOSFETs.

II. CYLINDRICAL GAA-FET

The two dimensional cross sectional view of the structure is shown in the below figure-

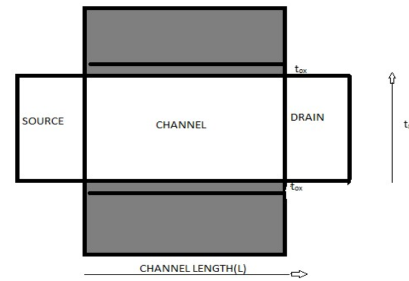

Fig.1.Cylindrical GAA MOSFET

The above figure shows the schematic structure of cylindrical gate all around MOSFET which is used for simulation. In the above figure the radial and lateral direction of the channel are shown to be along the radius and z-axis of the cylinder.

Where,

t_{ox}=thickness of gate oxide

t_{si}= thickness of silicon

L=length of the channel

Cylindrical gate all around MOSFETs are the type of multigate transistors in which the gate oxide and gate electrode is wrapped around the channel region and shows excellent electrostatic control of the channel,better scaling options, ideal sub-threshold swing as compared to other multigate transistors[7].Hence the CGAA MOSFETs are an excellent solution for nanoscale technology CMOS devices. However the cylindrical gate all around (CGAA) MOSFETs is one of the new technologies which further enables the scaling without hampering the device performance, due to higher drive current. Shorter cylindrical GAA MOSFETs can achieve higher packing density as compared to other multigate transistors.[2]

III. DERIVATION OF SURFACE POTENTIAL FOR CGAA FET

The potential distribution ϕ(r,z) in the channel region is obtained by solving the following 2-D Poisson's equation in cylindrical coordinate system[8].The two dimensional cross sectional view of the structure is shown in the below figure.

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial}{\partial r}(\phi(r,z))\right)+\frac{\partial^2}{\partial z^2}(\phi(r,z))=\frac{q\times N_a}{\epsilon_{si}} \quad (1)$$

The potential distributions inside the channel regions are approximated by a parabolic polynomial as-

$$\phi(r,z)=c_0(z)+c_1(z)r+c_2(z)r^2 \quad (2)$$

the coefficients c_0,c_1,c_2 are the functions of z only and can be determined by using the given boundary conditions.

$$\phi(0,0)=V_{bi} \quad (3)$$

$$\phi(0,L)=V_{bi}+V_{ds} \quad (4)$$

where V_{ds} is the drain to source voltage and V_{bi} is the built in potential between the source/drain and Si channel junction and is given by

$$V_{bi}=\frac{KT}{q}\ln\left(\frac{N_a\times N_d}{n_i^2}\right) \quad (5)$$

If we put r=0 in equation 1 then it will give us the center potential as given below-

$$\phi(r,z)|_{r=0}=c_0(z) \quad (6)$$

$$\phi(0,z)=\phi_c(z)=c_0(z) \quad (7)$$

where $c_0(z)$ will be the center potential and is a function of z only.the electric field at the center of the film is zero

$$\frac{\partial}{\partial r}\phi(r,z)|_{r=0}=0 \quad (8)$$

The electric field at the silicon interface is given by

$$\frac{\partial}{\partial r}\phi(r,z)|_{r=t_{si/2}}=\frac{\epsilon_{ox}}{\epsilon_{si}}\frac{(V_{gs}-V_{fb}-\phi(r,z))}{t_{ox}} \quad (9)$$

where ϵ_{ox} and ϵ_{si} are the permittivity of SiO_2 and Si respectively and V_{fb} is the flat band voltage.

Now,by differentiating equation 2 with respect to r and equating it with equation 8 we can get-

$$c_1(z)=0 \quad (10)$$

Further putting equation 10 in equation 2 we can get

$$\phi(r,z)=c_0(z)+c_2(z)r^2 \quad (11)$$

Then solving the above equation and using the given boundary conditions the value of $c_2(z)$ can be calculated.

Finally the center potential can be calculated by calculating the potential at r=0

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial}{\partial r}(\phi(r,z))\right)|_{r=0}+\frac{\partial^2}{\partial z^2}(\phi(r,z))|_{r=0}=\frac{q\times N_a}{\epsilon_{si}} \quad (12)$$

So,finally solving the above equation at r=0 we can get the center potential as shown below

$$\phi_c(z)=\left(\sqrt{\frac{4}{\lambda}}z\right)+\text{Bexp}\left(-\sqrt{\frac{4}{\lambda}}z\right)+\left((V_{gs}-V_{fb}-\frac{\lambda q N_a}{4\epsilon_{si}}\right)$$

(13)

By using equation 3 to 7 we can find the relationship between the center potential and the surface potential $\phi_s(z)$.

$$\phi_s(z)=\phi_c(z)+(V_{gs}-V_{fb}-\phi_c(z))\frac{t_{si}^2}{\lambda} \quad (14)$$

For the calculation of surface potential we need the value of z_{min} so in order to calculate the value of z_{min} we need to differentiate the center potential equation and equate it to zero[11].

Hence the value of z_{min} is given as-

$$Z_{min}=\sqrt{\frac{\lambda}{16}}\ln\left(\frac{B}{A}\right) \quad (15)$$

Now putting the value of z_{min} in above equation 14 we get surface potential as

$$\phi_s=(V_{gs}-V_{fb})+\left(2\sqrt{AB}-\frac{\lambda q N_a}{\epsilon_{si}4}\right)\left(1-\frac{t_{si}^2}{\lambda}\right) \quad (16)$$

IV. RESULTS AND DISCUSSIONS

In this section we are going to discuss the results which is obtained from the theoretical model of CGAA and compare the surface potential value with channel length for different varying parameters like gate oxide, temperature, channel doping, drain to source voltage and drain to gate voltage.

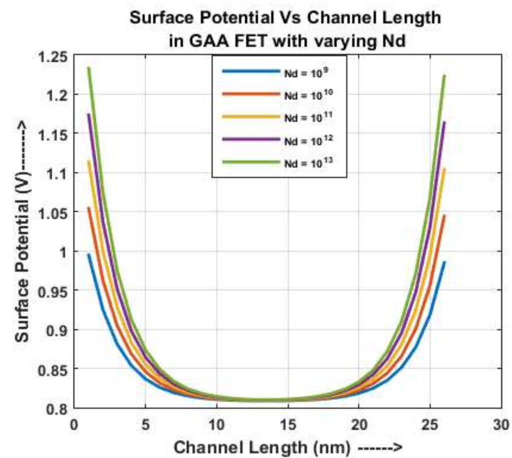

Fig.2-Surface potential vs Channel length for diferent doping concentration

Figure 2 shows the variation of the surface potential along the channel length(ranging from 1-25nm) with five different value of channel doping(ranging from 10^9-$10^{13}cm^{-3}$).

From the above figure we can conclude that as the doping concentration value is increased there is shift(i.e there is increase)in the value of surface potential.Initially for all the doping concentration value the surface

potential decreases till 20nm and after 20nm the potential value increases giving a parabolic curve.

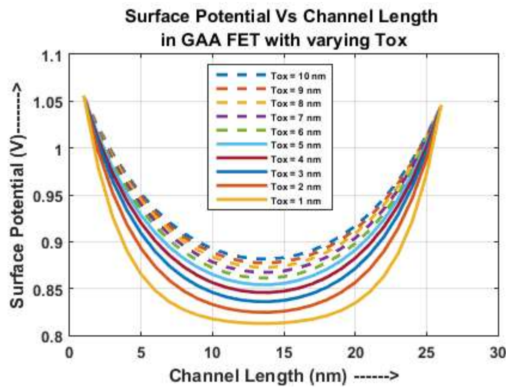

Fig.3-Surface potential vs Channel length for diferent oxide thickness(t_{ox})

Figure 3 shows the variation of the surface potential along the channel length(ranging from 1nm-25nm) with different value of oxide thickness.The effect of gate oxide thickness over the channel potential is that as gate oxide thickness is reduced,the gate control over the device increases.Thus scaling down of oxide thickness reduces the short channel effects.

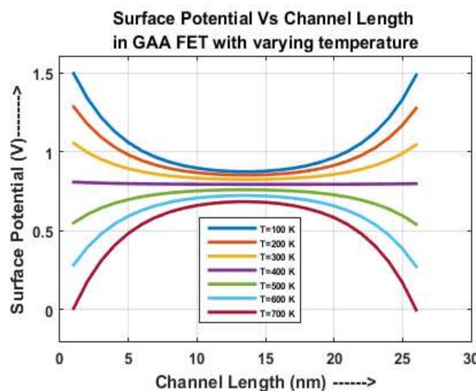

Fig.4-Surface potential vs Channel length for diferent temperature

Figure 4 shows that when we are applying smaller temperature value(that is till 300K) till 15nm channel length the value of surface potential tends to decrease and then it gradually increases giving the parabolic curve but after 500 K temperature we get the downward parabolic curve and surface potential value is increased till 0.8V after that the value decreases.

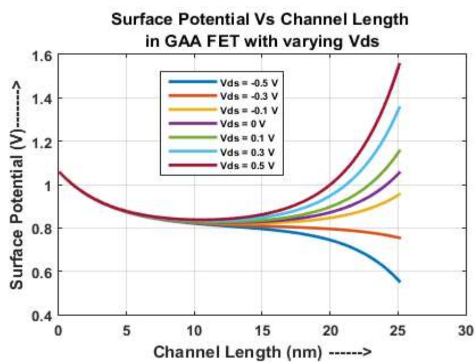

Fig.5-Surface potential vs Channel length for diferent V_{DS}

From the above figure we can conclude that till 15nm of channel length when we are increasing the value of V_{DS} the value of surface potential is decreasing, but after 15nm technology with increase in the value of V_{DS} there is increase in value of surface potential.

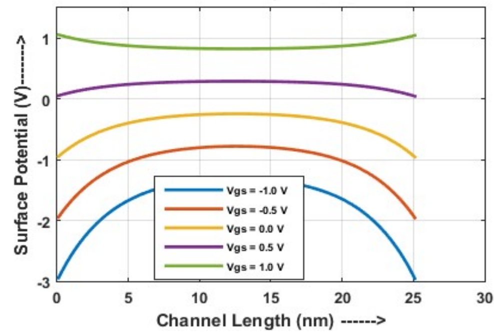

Fig.6-Surface potential vs Channel length for diferent V_{GS}

From figure 6 we can conclude that with increase in the value of V_{GS} there is increase in the value of surface potential.

V. CONCLUSION

An analytical potential model for the Cylindrical GAA MOSFETs using parabolic approximation of the channel is developed.Also the surface potential distribution of the Cylindrical GAA MOSFETs based on Poisson's equation is derived using the specific boundary condition.In this paper we studied the variation of the surface potential along channel length ranging from 1 to 25nm for different parameters like Temperature,Gate Oxide thickness,doping concentration,drain to source voltage etc.The oxide thickness should not be scaled down to very small values because tunneling problem through the oxide increases which hampers the device performance.

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