Design and Implementation of a Cyclic Analog to Digital Converter Architecture using Variable Range Flash ADC

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Abstract: The paper presents a unique design based on cyclic analog to digital conversion using a variable range flash ADC (Analog to digital Converters). The most important feature of the proposed design is that, a 4-bit conventional flash type ADC requires 15 comparators for its implementation whereas this model employs only four comparators to realize a 4-bit resolution. A feedback path is employed for a generation of 2-bit in each cycle. The design is being simulated using MULTISIM software. This architecture, if fabricated in IC form, can be a low cost less power alternative to conventional flash ADC architectures with a high resolution at a high speed with reasonably good accuracy, though requiring less area and consuming less power.

Index Terms: Analog to Digital Converters, Flash ADC, Cyclic ADC, Adaptive Flash ADC and Comparators.

I. INTRODUCTION

Signals in the real world tends to be analog, in order to process them with a digital circuit, we need to convert them to digital signals. Analog to digital converter is a device that converts a continuous analog signal (usually voltage) into its equivalent discrete form. The conversion in an ADC takes place in three different stages namely sampling, quantizing and encoding. In sampling process, the rate at which the sample of the parameter are to be taken depends on the most varying signal and it is necessary to sample this parameter at a rate faster than the fastest varying signal. The peak to peak amplitude range can be divided into the number of labels through quantization and the levels are known as quantizing level and finally the output after quantization is converted into coded form through encoding **[1-2]**.

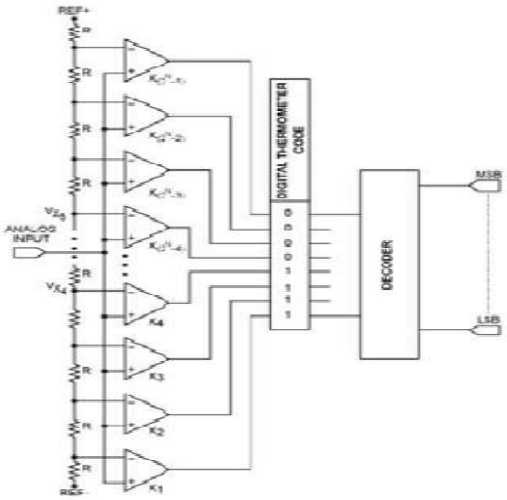

Fig.1. Conventional Flash ADC

Flash type analog-to-digital converters (ADCs) are the fastest way to convert an analog signal to its digital equivalent. They are ideal for large bandwidth applications. It is made by cascading high-speed comparators. The outputs of the comparators are a thermometric code which is fed to a priority encoder. The output code can be determined in one complete cycle. Flash ADCs contain an analog reference voltage with which the input analog voltage is compared. The digital output tells what fraction of the reference voltage is the input voltage. The reference voltage for the A/D converter may be provided internally or by an external source **[5-7]**. Since the accuracy of the output is directly affected by the reference voltage, it is important that the reference voltage should be stable and accurate during conversion. The number of bits that represents the digital output determines the resolution of the flash ADC. How closely the digital output approximates the input analog voltage also depends on the ADC resolution. The flash architecture uses a set of 2n-1 comparators to directly measure an analog signal to a resolution of n bits. Each comparator is biased to compare the input voltage to a discrete transition value **[8-9]**.

However, they typically consume more power than other ADC architectures and its resolution is normally limited to 8-bits and can be quite expensive. This limits them to high frequency applications that typically cannot be

addressed any other way. The tradeoff for practical application of a flash ADC is its circuit complexity and number of bits, i.e., resolution.

Though the speed of flash ADCs is high, its accuracy is medium **[3].**

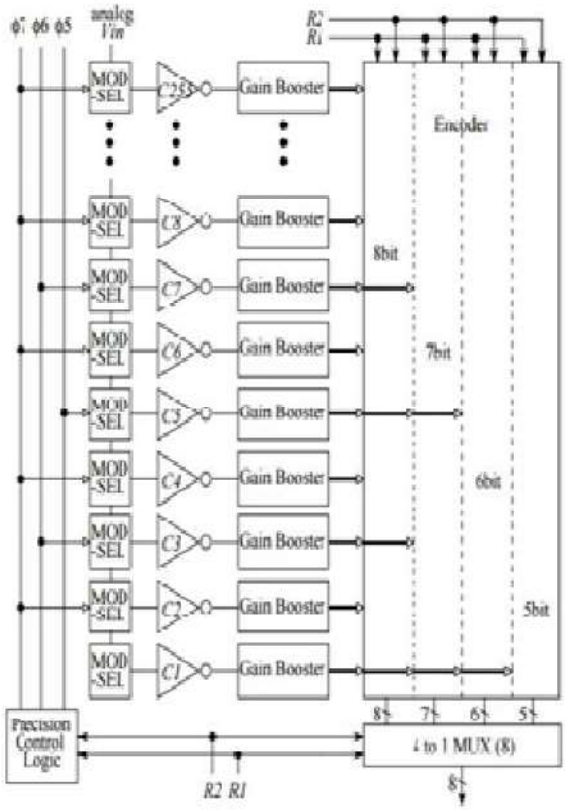

Fig.2. Adaptive Flash ADC

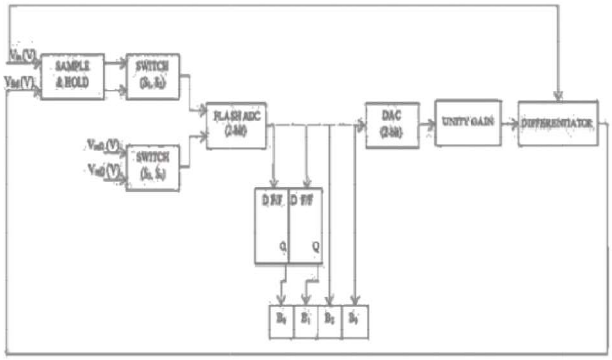

Fig 3. Block diagram of an adaptive type variable range flash ADC.

Adaptive Flash ADC has an active mode and a standby mode in which switches work alternatively. In the active mode, one switch is connected to the analog voltage which is fed to the comparator. Similarly, in the standby mode the other switch is connected to the standby voltage which is passed to the comparator. The analog input voltage varies between ground and Vdd, but the standby is fixed to either ground or Vdd **[4].**

Therefore, it is observed that in conventional Flash ADC as the resolution increases the number of comparators increases to a large extend. Also in Adaptive Flash ADC, though the number of comparators were reduced but the difficulty of using manual switching existed. So to avoid these two problems this proposed architecture is designed and implemented.

II. METHOD OF APPROACH

The complete block diagram of an adaptive type variable range flash ADC which is proposed in this paper is shown in **Fig3.**

The analog input signal (Vin) and feedback voltage (Vfed) is fed to switch S1 and S2 respectively through sample and hold circuit. The sample and hold circuit will sample and hold the signal for a given period of time and it will produce a delay for getting the other bits from feedback cycle. The reference voltages (Vref1) and (Vref2), whose values are 4V and 1V are fed to switch S3 and S4 respectively for getting 4-bit output. For getting first 2-bit, two switches Vin and Vref1 will be high and the output of the switch will have fed to 2-bit Flash Type ADC. In Flash ADC the reference voltage is compared with the analog input voltage. When the analog voltage exceeds the reference voltage, the comparator generates logic High as output meanwhile if the analog voltage is less than the reference voltage the comparator generates logiclow output. Depending upon the output of the comparator the corresponding priority encoder will generate the required 2-bit output. This 2-bit will go through the D-Flip Flop and is fed to the Digital to Analog Converter. The D-Flip Flop will give the delay for getting another 2-bit. Digital to Analog Converter (DAC) will convert the 2-bit signal into its analogous value. The analog output is fed to unity gain so as to get a positive analog value. The output of the unity gain is fed to a differentiator, which is used for calculating the difference between the analogous voltage from the DAC output and the input analog voltage (Vin). The output of the differentiator is being fed to the ADC (Vfed) and the reference voltage (Vref2) will be high and goes to the 2-bit. Flash Type ADC and subsequently the other 2-bit is obtained. Likewise, the output for higher bit ADC can be fetched.

III. SIMULATIONS AND RESULTS

The proposed architecture is simulated with a resolution of 4-bit. The design gives digital output for any analog input within a single clock pulse. The output bit pattern is fed through a DAC to reconstruct the signal and this reconstructed signal is compared to the original input using an oscilloscope. The complete simulation in Multisim is shown in **Fig 4.**

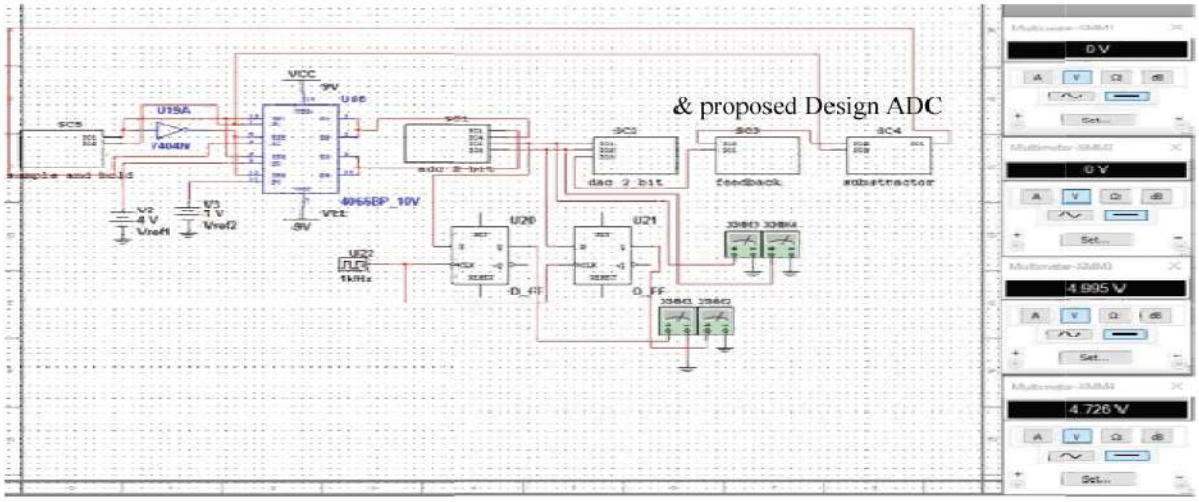

Fig 4: Simulink model of the proposed Design using Multisim

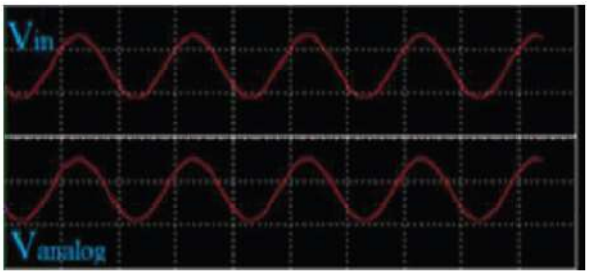

Fig.5. V_{in} Vs V_{analog}

Fig. 5 depicts the comparison of the input analog voltage which is fed to the 2-bit sub-ADC and the output analogous voltage from the DAC. Both are compared and found to be similar with each other.

A comparative analysis has been done between the proposed flash ADC and the conventional flash ADCs. **Table 1** below shows the comparison based on some important parameters like resolution, power consumption, complexity, speed and its economic benefits.

Table 1: Comparison Between Conventional ADC & proposed Design ADC

Sl. No	Parameters	Conventional ADC	Proposed ADC
1	**Resolution**	good	better
2	**Power Consumption**	more	less
3	**Speed**	Same	same
4	**Complexity**	more	less
5	**Economics Benefit**	255 comparators for 8-bit resolution	8 comparators for 8-bit resolution

IV. CONCLUSION

In this paper, an effective and simple architecture of a variable range adaptive flash ADC is being shown. The maximum number of bits displayed in the proposed architecture is 4 bits, which works properly for a feedback voltage of less than 1V when V_{refl} is 4V. The Simulation results confirm the validity of the proposed design.

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