Cascade Multilevel Inverter with Single DC Source and Low Frequency Three Phase Transformers for High Power Applications

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Abstract: It is difficult to connect a single power semiconductor switch directly to medium voltage grid. For these reasons a new family of multilevel inverters has emerged as a solution to work with higher voltage level. Multilevel inverters are known have output voltage with more than two levels. As a result the inverter out voltages have reduced harmonics distortion and high quality of wave forms .Additionally the devices, are confined to fraction of DC link voltage. These characteristics make multilevel inverter to adopt for high power & high voltage applications. Cascade multilevel inverter (CMI) is one of the productive topology from multilevel family.CMI features a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure and modulation. Therefore, in case of fault in one of this module, it is possible to replace it quickly & easily. Moreover with appropriate control strategies it is possible to bypass the faulty module without stopping the load. In the preset work we have investigated different CMI based technologies with separate & single DC source.

Keywords - Cascade multilevel inverter (CMI), Neutral point converter (NPC), Pulse width modulation (PWM)

I. INTRODUCTION

Recently, R&D in multilevel converters and their applications have been very visible in the literature. Particularly while systems are dealing with utility applications, transformer coupling often becomes essential. Such features are observed in Neutral point converter (NPC). In general numerous transmission and distribution systems are facilitated with NPC employing zigzag transformers. This class of converter is highly preferred because of the lower harmonic content and improved power quality aspects. In fact NPC with zigzag transformer size is quite larger because large numbers of components are utilized. However, in spite of that archetype, presented converter can effectively replace in such areas. This is because present CMI is coupled with low frequency three phase transformers. Further in presence of PWM operation, voltage and current waveforms are almost equal to that of NPC converters performance. All these features facilitate the converter to operate perfectly for utility applications.

II. PROPOSED CMI WITH SINGLE DC SOURCE BY USING THREE PHASE TRANSFORMERS

These classes of converters are extensively used in utility interfacing applications. But these structures utilize the single phase transformers for each H-Bridge, which makes the converter size big and thereby increasing the cost. Fig. 1 demonstrates H-Bridge multilevel inverter with single dc source and several low frequency three phase transformers, this make the size of the equipment come down with less price tag.

Now, coming to structure point of view, each primary terminal of the transformer is connected to an H-Bridge module so as to synthesize output voltages of +VDC, Zero, -VDC. Every secondary of transformer is connected in series to enhance the output voltage level. Further, each phase terminal is delta connected to restrain the third harmonic component. Fig. 1 expresses that, primary of each phase is three phase and secondary is single phase terminal. All three terminals are series connected to generate phase voltage. Therefore, each phase can be expressed independently. As a result each phase multilevel inverter can be depicted as an isolated H-Bridge cascaded multilevel inverter. We can obtain the relation between input and output voltages of three phase transformer as

$$\begin{bmatrix} V_{AK}; V_{BK}; V_{CK} \end{bmatrix} = N \begin{bmatrix} T \end{bmatrix} \begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix}$$

Vak, Vbk,Vck are primary terminal of phase "a", phase "b" and phase "c" Where, T is transformation matrix and defined as

$$T = \begin{bmatrix} 2/3 & -1/3 & -1 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix}$$

Similarly, N is the transformation ratio (n2/n1) between primary and secondary and if there is a balanced input, then sum of each phase voltage would become zero

$$V_{ak} + V_{bk} + V_{ck} = 0$$

Proposed multilevel inverter using three-phase transformer (fig-1)



$$\begin{bmatrix} V_{Ak} \\ V_{Bk} \\ V_{Ck} \end{bmatrix} = N \begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix}$$

From previous relation CMI with three-phase configuration, we are obtaining each phase output voltage of transformer as product of input voltage and transformation matrix N. But under unbalanced condition, equation (4.4) is not satisfied because primary of transformer is connected to an H-Bridge cell generating Vdc, zero, -Vdc. So, the output voltage of Vak, Vbk, and Vck are equal to Vdc. Thus summation of three voltages is not equal to zero; due to this fact output voltage is unbalanced. However, equation (4.1) holds good for all conditions. In other terms, we can generate voltages at Vak=VDC, Vbk=-VDC, and Vck=0. Summation of such voltages will result to zero. However, the fundamental idea behind this is, magnetic circuit concept, notifying that flux at the primary of phase "a" will be equally influenced on phase "b" and phase "c" and becomes -1, so unbalanced relationship is also included in equation (4.1). As shown in Fig.4.1, proposed multilevel inverter secondaries[1]-[5] are connected in series so that the output is the sum of three voltages. Thus it can be represented as

$$\left[V_{AS}; V_{BS}; V_{CS}\right] = \left[\sum_{i=1}^{k} V_{Ai}; \sum_{i=1}^{k} V_{Bi}; \sum_{i=1}^{k} V_{Ci}\right]$$

Herein, output voltage VAS is defined as summation of phase "a" voltages i.e. VA1+VA2+VA3. In a similar fashion corresponding summation will produce VBS and VCS. Further, to confirm the proposed CMI working pattern, output voltage characteristics are examined in the next section.

III. OUT PUT VOLTAGE CHARACTERISTIC

Output voltage of the three-phase transformer will be determined by combination of A, B and C voltages and there are three possibilities in output voltage of transformer. Switching pattern of each phase and output voltage of each transformer is shown in Fig. 2. It is to be noted that, presented voltages are resultant voltages of phase "a" and such voltages are obtained by summation of three voltages i.e Vak, Vbk and Vck. However, Output voltage of proposed inverter is sum of secondary terminal voltages of transformer, which are connected in series and all these are independent of switching range from $0 < \alpha k < \pi/2$. From Fig.2, output voltage of phase "a" (VA) is figure out to be symmetrical in nature. In general form, Fourier expression can be written as:



Fig.2 Details of switching pattern and output voltage waveform characteristics for CMI with three-phase transformers

Where bnk is a constant.

Output characteristics of phase "a" voltage can be obtained between three switching ranges i.e $0 \le \alpha k \le \pi/6$, $\pi/6 \le \alpha k \le \pi/3$, $\pi/3 \le \alpha k \le \pi/2$. And these are shown in Fig.2.

For case-1 i.e. $0 \le \alpha k \le \pi/6$, $\pi/6$:

$$b_{nk} = \frac{4V_{dc}}{\pi} \begin{bmatrix} \int_{a_k}^{\frac{\pi}{3} - a_k} \sin(n\theta) \, d\theta + \frac{3}{3} \int_{\frac{\pi}{3} + a_k}^{\frac{\pi}{3} + a_k} \sin(n\theta) \, d\theta \\ + \frac{4}{3} \int_{\frac{\pi}{3} + a_k}^{\frac{\pi}{2}} \sin(n\theta) \, d\theta \end{bmatrix}$$

i.e. $b_{nk} = \frac{4V_{dc}}{n\pi} \cos(n\alpha_k)$ ----(1)

For case-2, i.e. $\pi/6 \le \alpha k \le \pi/3$, $\pi/3$;

$$b_{nk} = \frac{4V_{dc}}{\pi} \begin{bmatrix} \int_{\pi/_{j}-a_{k}}^{a_{k}} \sin(n\theta) \, d\theta + \frac{3}{3} \int_{a_{k}}^{2\pi/_{j}-a_{k}} \sin(n\theta) \, d\theta \\ + \frac{2}{3} \int_{2\pi/_{j}-a_{k}}^{\pi/_{j}} \sin(n\theta) \, d\theta \end{bmatrix} \quad -----(2)$$

 $b_{nk} = \frac{4V_{dk}}{n\pi} \cos(n\alpha_k).$

For case -3, i.e. $\pi/3 \le \alpha k \le \pi/2$

$$b_{nk} = \frac{4V_{4k}}{\pi} \left[\int_{a_k - \frac{\pi}{3}}^{2\pi/3 - a_k} \sin(n\theta) \, d\theta + \frac{2}{3} \int_{a_k}^{\pi/2} \sin(n\theta) \, d\theta \right] \quad ----(3)$$

$$b_{nk} = \frac{4V_{dc}}{n\pi} \cos(n\alpha_k)$$

From equations (1,2,3), Fourier progression[21]-[25] is same. In a similar fashion Fourier transform for primary voltages of transformer Vak, Vbk, Vck are given as

$$\begin{split} V_{ak} &= \sum_{n=1}^{\infty} b_{nk} \sin(n\theta) \\ V_{bk} &= \sum_{n=1}^{\infty} b_{nk} \sin(n\theta - \frac{2n\pi}{3}) \\ V_{ck} &= \sum_{n=1}^{\infty} b_{nk} \sin(n\theta + \frac{2n\pi}{3}) \end{split}$$

Which are 1200 apart from each phase and coefficients of bnk and Vak are half wave symmetries, henceforth odd function can be written as

$$b_{nk} = \frac{4V_{dc}}{n\pi} \cos(n\alpha_k)$$

Using equation (1), output phase voltage of VAK can be expressed as:

$$V_{AK} = \sum_{n=1}^{\infty} b_{nk} \sin(n\theta) - 1/3$$
$$\times \sum_{n=1}^{\infty} b_{nk} \left(\sin(n\theta) + 2\sin(n\theta)\cos(\frac{2n\pi}{3}) \right)$$

In above equation if n=3, 9...3(p-2), 3p, then equation becomes zero i.e.

$$V_{AK} = 0$$

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And if n=1, 5, 7, 11..., p, then equation becomes

$$V_{AK} = \sum_{n=1}^{\infty} b_n \sin(n\theta)$$

Thus least harmonics in output waveform will be 5, 7, 11, p-2, p.

IV. PERFORMANCE VERIFICATIONS

Performance of the proposed architecture is verified by using three major switching techniques namely; fundamental frequency, selective harmonic elimination. The main idea behind the operation with different techniques is to explore the potential of the proposed CMI. However, to verify the performance of the proposed CMI, prototype experimentation[6]-[10] is carried out in the laboratory and adequate results are presented to confirm the findings.

(A) **Fundamental Frequency Approach**

Before proceeding, let's compare the output waveform characteristic of conventional CMI and the proposed with three-phase transformers. This is CMI demonstrated in Fig.3 (a). However, conventional converter characteristic waveform and its switching fashion is quite different when compare to the proposed one. Note that, three single phase transformer produce seven level output waveform by using three switching angles. In fact, minimum harmonic switching angle can be easily solved by the Newton-Raphson approach and this kind of approach is observed in numerous publications. Later, Fig.3 (b) gives the details of output characteristics of CMI with three-phase transformers and output waveform. At this point one should observe that switching criterion is quite different and in particular Fig.3 (b) provides the characteristics at each transformer terminal in phase "a". Thus one can finds the difference between the conventional switching and proposed switching. However, mathematical verifications are already done in preceding sections.

To demonstrate the fundamental frequency approach, consider the theoretical output voltage waveforms VA1, VA2 and VA3 of each of the three-phase transformers[16]-[20]. The output voltages are connected in series to produce a net output voltage i.e. VA1+VA2+VA3 and this situation is shown in Fig.3 (b). Output characteristics shown in Fig.3 (b) . The phase voltage VA1 is obtained by three input voltages i.e. val, vb1 and vc1 (observe Fig.1). In a similar fashion VA2 and VA3 can be obtained. As far as concerned these output voltages are independent of switching angles, range from $0 < \alpha k < \pi/2$. So output voltage can be represented as:



Fig.3 Details of waveforms for (a) conventional seven level inverter,

(B) Multilevel Selective Harmonic Elimination PWM Technique

The multilevel SHEPWM technique[11]-[15] has a theoretical potential to achieve the highest output power quality at low switching frequencies in comparison to other methods. Due to mathematical complexity SHEPWM is less preferred. But still this method is effective in suppressing significant harmonics in the system. Applying SHEPWM to multilevel converter is well presented by several authors . But in present case we adopt this technique to the CMI with three-phase transformers.

V. EXPERIMENTAL RESULTS

(A) Fundamental Frequency Approach

Switching is carried out with three switching angles per quarter period. Fig.4. provides the experimental results.

of the proposed CMI. For simplicity, results of phase "a" only are presented. All the waveforms for parallel connected resistive and inductive loads (400 Ω + 1000 mH) were taken at the modulation indexes 1.0, 0.5 and 0.2 respectively. Observing Fig.4 at modulation index 1, we can notice that 13 level performances are achieved with just nine H-bridge cells. This defines the inherent potential converter. In fact this is an important finding regarding the proposed CMI.



Fig.4 Performance of the proposed cascaded multilevel inverter with by using fundamental frequency approach at modulation index 1, 0.5, and 0.2 (from top to bottom)

(C) Selective Harmonic Approach



Fig.5 Performance of the proposed cascaded multilevel inverter with by using selective harmonic PWM approach at Modulation index 1 ,0.5, 0.2 (from top to bottom)

VI. CONCLUSION

This paper presented a new version of cascaded multilevel inverter, which employed a single dc input source and low frequency three-phase transformers. Performance of the proposed CMI is investigated with three switching techniques namely, fundamental frequency switching and selective harmonic elimination PWM approach.

REFERENCES

- [1] Fazel SS, (2007) Investigation and comparison of multi-level converters for medium voltage applications. Ph.D. Thesis, Berlin Technical University.
- [2] Baker RH, (1980) High-voltage converter circuit. US Patent 4203151.
- [3] Meynard TA, Foch H, Forest F, Turpin C, Richardeau F, (2002) Multi-cell converters: derived topologies. IEEE Transact ions on Industrial Electronics, vol.49, no.5:978–987.
- [4] J.-S. Lai and F. Zheng Peng, "Multilevel converters-a new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, no. 3, pp. 509–517, May 1985.
- [5] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, B Multilevel converters a survey, in Proc. Eur. Power Electron. Conf., Lausanne, Switzerland, 1999.
- [6] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, B Multilevel converters for large electric drives,

IEEE Trans. Ind. Appl. , vol. 35,pp. 36–44, Jan./Feb. 1999.

- [7] J. Rodriguez, J.-S. Lai, and F. Z. Peng, B Multilevel inverters: A survey of topologies, controls, and applications, IEEE Trans. Ind. Electron., vol. 49, pp. 724–738, Aug. 2002.
- [8] J. Rodriguez, B. Wu, S. Bernet, J. Pontt, and S. Kouro, B, "Multilevel voltage source converter topologies for industrial medium voltage drives, IEEE Trans. Ind. Electron. (Special Section on High Power Drives ,vol. 54, pp. 2930–2945, Dec. 2007.
- [9] M. Marchesoni, "High-performance current control techniques for application to multilevel high-power voltage source inverters," IEEE Trans. Power Electron., vol. 7, no. 1, pp. 189– 204, Jan. 1992.
- [10] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, B The age of multilevel converters arrives, IEEE Ind. Electron. Mag., pp. 28–39, Jun. 2008.
- [11] Meynard, T.A., and Foch, H.: 'Multi-level conversion: high voltage chopper and voltagesource inverter', IEEE-PESC Conf. Rec., 1992,pp. 397–403
- [12] J. K. Steinke, "Switching frequency optimal PWM control of a threelevel inverter," IEEE Trans. Power Electron., vol. 7, no. 3, pp. 487– 496, Jul. 1992.
- [13] Z. Pan, F.Z. Peng, K.A. Corzine, V.R. Stefanovic, J.M. Leuthen, and S. Gataric, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," IEEE Trans. Ind. Applicat., vol. 41, no. 6, pp. 1698– 1706, Nov. 2005.
- [14] B. Ozpineci, L.M. Tolbert, and J.N. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," IEEE Power Electron. Lett., vol. 3, no. 3, pp. 92–95, Sept. 2005.
- [15] A. Nabae, I. Takahashi, and H. Akagi, "A neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. 1A-17, no. 5, pp. 518– 523, Sept. 1981.
- [16] B.P. McGrath, D.G. Holmes, and T. Meynard, "Reduced PWM harmonic distortion for

multilevel inverters operating over a wide modulation range," IEEE Trans. Power Electron., vol. 21, no. 4, pp. 941–949, July 2006.

- [17] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: A practicable way to balance dc-link voltages," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 752–765, Aug. 2002.
- [18] Brendan Pete McGrath, Donald Grahame Holmes, "Multicarrier PWM Strategies for Multilevel Inverters," IEEE Trans. Ind. Electronics, vol. 49, no. 4, Aug 2002.
- [19] Tao Yu, Chaejoo Moon, Sungjun Park, SungGeun Song, Joungmin Lim, "A Study on Novel PWM HBML Inverter Using Commonarm," in IEEE International Conference on Industrial Technology (ICIT 2006)
- [20] Damoun Ahmadi, KeZou, Cong ,Yi Huang, and Jin Wang , " Universal Selective Harmonic Elimination for High Power Inverters," ," IEEE Trans. Power. Electronics, vol. 26, no. 10, Dec 2011.
- [21] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Scuitto, "A new multilevel PWM method: A theoretical analysis," IEEE Trans. Power Electron., vol. 7, no. 3, pp. 495–505, Jul. 1992.
- [22] Rajesh Gupta, Arindam Gosh," Contorl of cascaded transformer multilevel inverter based D-STATCOM," Elsevier, Electric power system research",vol. 77, pp. 989-999, 2007.
- [23] C. Wang, "Research on the topology, PWM algorithm and balance control of neutral point voltage in multilevel converters," Ph.D. dissertation, Tsinghua Univ., Beijing, China, 2008.
- [24] Tao Yu, Chaejoo Moon, Sungjun Park, Sung Geun Song, Joungmin Lim, "A Study on Novel PWM HBML Inverter Using Common-arm," in IEEE International Conference on Industrial Technology (ICIT 2006)
- [25] Feel-soon kang, Sung-jun Park, Man Hyung Lee, Cheul-U Kim, "An Efficient Multilevel-synthesis approach and its application to a 27-level inverter," IEEE Trans. Ind. Electronics, vol. 52, no. 6, Dec 2005.

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