Active Memory modules in Proposed Fault Tolerant Irregular Triangle Multistage Interconnection Network

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Abstract : Multistage Interconnection Networks (MINs) interconnect various processors and memory modules. The Systems with thousands of processors embedded attract the researchers in continuous improvement of different aspects of these MINs such as complexity, fault tolerance, performance evaluation, routing of data and control. In this paper a new class of Irregular Fault Tolerant MIN named as Triangle MIN has been introduced and studied. This MIN provides better Bandwidth, Probability of acceptance, Processing Power, Processor Utilizations, Through Put and Permutation passable without Faults and with Faults in the Network as compared to popular MINs like Quad Tree, Theta, Omega and Phi Networks.

Keywords Irregular Fault Tolerant MIN, Design of MIN, Routing, Performance Parameters, Permutation passable.

I. INTRODUCTION

In today's era the Computation Speed and Computation Power are increasing constantly. The MINs are used in important applications like ATM Networks, Weather Forecasting and in almost every field where instant response and complex calculations are required[7]. The MINs use more than one stage of small interconnection networks like Switching Elements (SEs)[1][9].Broadly there are two types of MIN namely static regular and irregular. If the MIN has same no of SEs in all the stages then it is called as regular MIN, otherwise it is called as irregular MIN. This paper introduces and analysis a new class of Irregular Fault Tolerant MIN named as Triangle MIN. On the basis of Performance parameters and Permutation Passability , the Proposed MIN has been compared with popular MINs like Quad Tree(QT), Theta(THN), PHI(PHN) and Omega Networks.

II. DESIGN OF TRIANGLE MIN

The Network is an Irregular Multistage Interconnection Network, of size N*N. It has N sources and N destinations. The MIN consists of n stages ($n=\log_2 N$).

The network Comprises of two identical groups of switching elements (SEs), named as G0 and G1.Each group incorporates N/2 sources and N/2 destinations. Both the groups are connected to the N inputs through N multiplexers, and to the N outputs through N no. of demultiplexers. The switches in all the stages are of size 3*3 except the last one. The switches in the stages n-3,n-2 and n-1 have been connected to each other through links called as auxiliary links. These links are used when the SE in the next stage is busy or faulty. This makes the network more fault tolerant and reliable.

The Triangle network of size 2^n*2^n consists of (2m-2) stages where $m=\log_2(N/2)$.This network has

(2^n -2) no. of switches of size 3*3 and 2^{n-1} no. of switches of size 2*2.Each source is connected to one switching element in each group with the help of multiplexers. The network of size 16*16 is shown in

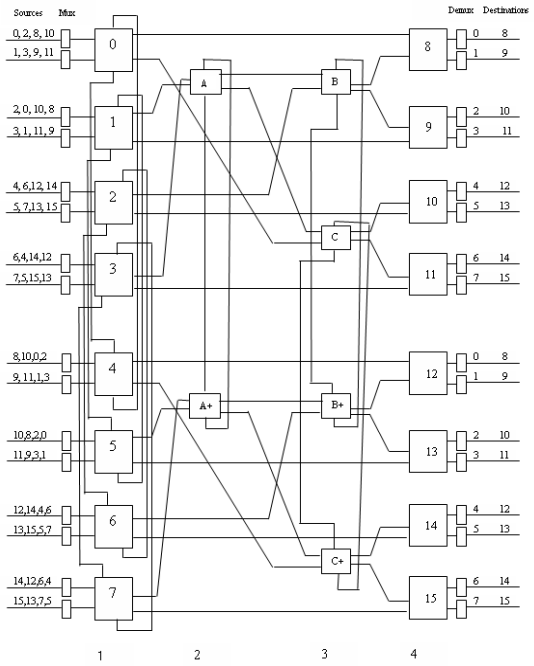

Fig 1 : Design of Triangle MIN

III. REDUNDANCY GRAPH

The Redundancy Graph is a pictorial representation of the architecture of a MIN. It shows all the possible paths from every source to every destination. [6][7]

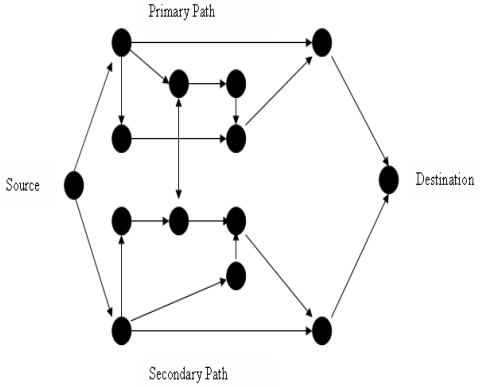

Fig 2 : Redundancy Graph of Triangle MIN

IV. ROUTING ALGORITHM

Let the source and destination in binary [11] be represented as

$S=S_{n-1}\ldots\ldots\ldots\ldots S_1S_0$

$D=D_{n-1}\ldots\ldots\ldots D_1D_0$

Algorithm

Step1 : Start

Step2 : The MSB of the destination address is checked and on the basis of it ,one of the sub networks G0 or G1 is selected.

Step3 : Let us suppose the address of the following SE is known. If the destination address is the address of this SE ,then the shortest path is used and the further routing is not required as the data has reached the destination.

Step4 : If the SE is busy then route the data to auxiliary SE through auxiliary links. If this is also busy then drop the request. Otherwise go to step 5 .

Step5 : The secondary path is selected .Set MSB of the routing tag as 1.The bits of the destination will make the data to reach the destination through intermediate stages. If the SE in any of the stages except the last one , is busy go to step 5

Step6 : Route the data [6] to auxiliary switch in the same stage (Route the data to auxiliary switch in the previous stage in case of faulty SE)

Step7 : Bit D_0 of the routing tag will guide the data through a particular demultiplexer and the destination will be reached.

Step8 : Stop

V. FAULT TOLERANCE AND REPAIR

If the network is able to work, of course with degraded efficiency, in the presence of faults in critical components [4] then the network is called as fault tolerant. A network is single fault tolerant if it can work with full access in the presence of fault in single SE. If the network is able to provide connections from all sources to all destinations in the presence of k faults in the network [8] , then this network is called as k fault tolerant network.

The proposed MIN satisfies the fault tolerant criteria [10] [12] because it can work in the presence of certain faults. If there is fault in the primary path then secondary path will be chosen for routing the data. Moreover there are multiple paths from one type of source to one type of destination which makes this network more Fault Tolerant and reliable as compared to other existing networks like Quad Tree, Theta and Phi Networks.

Moreover the auxiliary links [2] in all the stages except the last one provides the alternate route of the data. The critical case is when the fault is present in the SE in same loop. In this case certain pair of source and destination shall be disconnected.

Theorem 1 : Different path lengths are available for routing from source to destination in primary and secondary routes**.**

Proof: The probability of request forwarding within stages of the Triangle Network is different. Moreover the auxiliary links are available in all the SEs in all the stages except the last one. If fault in any of these SE happens then the data will be routed to the auxiliary SE in the same stage through auxiliary links.

Theorem 2 : The Triangle Network disconnects some source from some destination in the presence of fault in both the auxiliary switches in the same stage.

Proof : Let us suppose Source S is guided through a Faulty Switch to destination D. If the auxiliary switch in the same stage is also faulty then source S gets disconnected from destination D.

Lemma 1 : Triangle Network maintains the connectivity in the presence of the fault only if the auxiliary switching element in the same stage is Fault Free.

Repair : To rectify, just replace the loop engaged in the faulty components with the new one.

VI. EXPERIMENTAL RESULTS ON PERFORMANCE PARAMETERS

The Triangle Network has been analyzed on the basis of following parameters.[7][15][3]

6.1 Bandwidth(BW)

It is defined as average number of active memory modules in a transfer cycle of the Interconnection Networks. The bandwidth of a^n*b^n (a^n no of sources and b^n no of destinations) Network is calculated as

Bandwidth = $b^n * Pn$,where Pn is the probability of requests being forwarded.&P_0=P

For any stage of a MIN ,the output rate of request q is a function of its input rate and is given by

$q = 1-(1-p/b)^a$

The equations derived for The Triangle Network are

(1) $P[1]= 1-(1-P[0]/3)^3$

(2) $P[2]=1-(1-P[1]/4*3)^3$

(3) $P[3]=1-([1-2 * P[2]/3][1-P(1)/4*3])^3$

(4) $P[4]=1-\{(1-P[1]/2)* (1-P[3])\}^2$

Let us discuss how these equations have been derived .

First stage is getting N no of requests. The switches size is 3*3.The probability of forwarding the requests from switches of first stage to second stage is ¼ and switches are of size 3*3 . The double than the second stage switches have been used in the third stage so the probability of requests from second stage is double and from first stage is ¼ . The final stage is getting ½ no of requests from first stage and double no of requests from

the third stage. The switches in final stage are of size 2*2 .

6.2 Probability of Acceptance (Pa)

It is defined as ratio of bandwidth to the expected no of requests generated per cycle.

(1) $Pa=BW/a^n*p$ req gen

6.3 Processor Utilization(PU)

It is defined as percentage of time the processor is active doing computation without accessing the global memory.[5]

(1) $PU=BW/a^n*p$ req gen $*T$,

where T is average time used for a memory or read/write operation.

6.4 Processing Power(PP)

It is defined as sum of processor utilization over the number of processors.[13][7]

(1) $PP=a^n*PU$

6.5 Throughput

It is defined as maximum amount of data delivered per unit time

(1) Throughput = PU*p req gen

The table 1 has been designed on the basis of the formulas discussed in section 6.Here Probability of request generation (Preq.gen) at the source side of the network is used from 0.1 to 1.0 to calculate the Performance Parameters of Triangle MIN.

Table 1 : Performance Parameters of Triangle MIN

Preq. gen	Bandwidth	Probability of acceptance	Processor Utilization	Processor Power	Throughput
0.1	3.46942	2.16838	0.61953	9.91248	0.99124
0.2	6.07446	1.89826	0.54236	8.67776	1.73555
0.3	8.06673	1.68056	0.48016	7.68256	2.30476
0.4	9.55772	1.49339	0.42668	6.82688	2.73075
0.5	10.72012	1.34001	0.38286	6.12576	3.06288
0.6	11.62353	1.21078	0.34593	5.53488	3.32092
0.7	12.32997	1.10089	0.31454	5.03264	3.52284
0.8	12.88769	1.00685	0.28767	4.60272	3.682176
0.9	13.33048	0.92572	0.26449	4.23184	3.80865
1.0	13.66272	0.85392	0.24397	3.90352	3.90352

The Fig 3,Fig 4,Fig 5,Fig 6,Fig 7 are using the values in table 1 for Triangle MIN.The same set of formulas have been used to calculate the Performance Parameters as discussed in section 6 for THN,QT and PHN.The study shows that all the performance parameters for Triangle MIN are better as compared to other MINs as shown in figures.

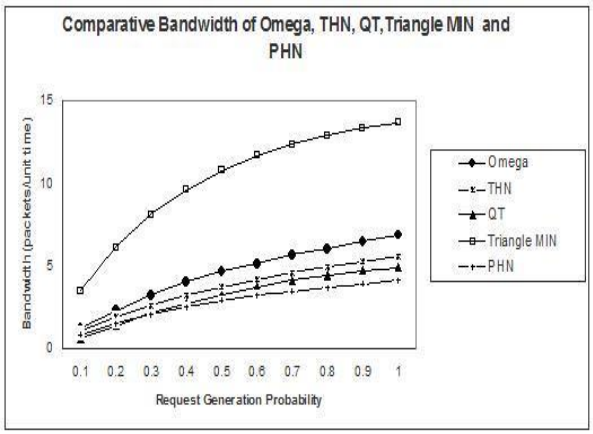

Fig 3

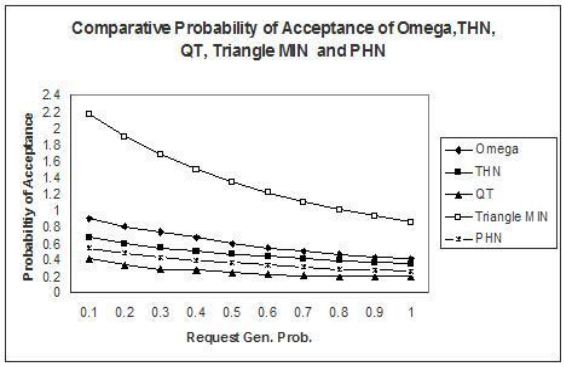

Fig 4

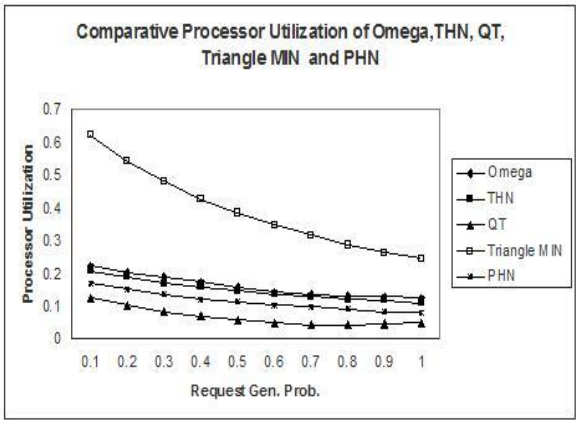

Fig 5

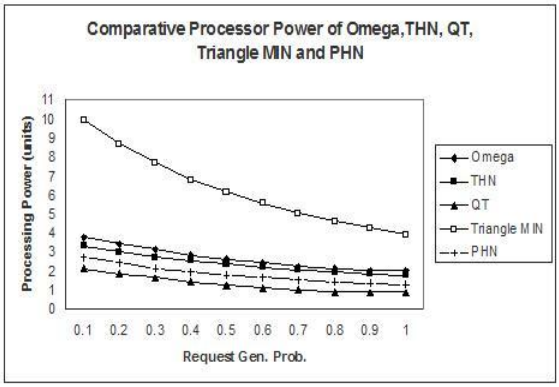

Fig 6

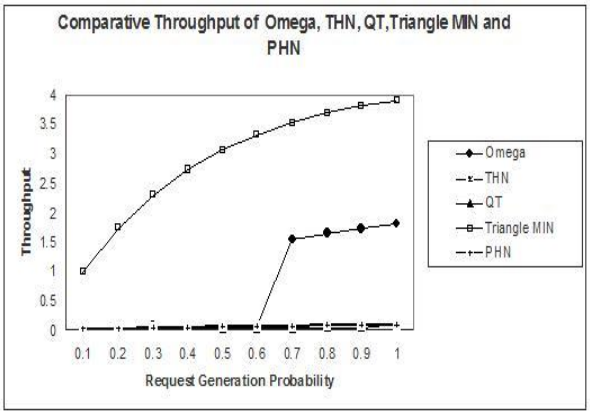

Fig 7

VII. PERMUTATION PASSABLE

It is a set of N data transfers, all of which are performed simultaneously in the network. The $\log_2 N$ stages network allows only some subset of N! passable permutations.

Let the source and destination in binary [11] be represented as

$S=S_{n-1}\ldots\ldots\ldots\ldots S_1S_0$

$D=D_{n-1}\ldots\ldots\ldots D_1D_0$

There are two ways to evaluate the Permutation Passability of the MINs.

7.1 Identical Permutation

It is one to one communication between same source and same destination.

$S_{n-1} \rightarrow D_{n-1}$, --------- , $S_o \rightarrow D_o$

7.2 Incremental Permutation

Here each source is connected to destination in a circular chain.[16]

Example $S_0 \rightarrow D_4$, …… , $S_{n-1} \rightarrow D_3$

We have considered two cases

I Non Critical (N-cr) It is a case when fault is present in a single switch.

II Critical (Cr) It is a case when fault is present in a loop

We have compared the proposed Triangle Network with other popular MINs on the basis of Incremental Permutation for 100% requests.

In the tables and figures discussed below n-cr stands for Non Critical case and cr stands for Critical case in the respective MINs. The incremental permutation of Omega Network has not been discussed because Omega Network is a regular network. It has static routing and has equal path lengths because of same no of switches in all the stages.

The table 2 shows the actual no of requests getting matured and their average path lengths for Triangle MIN.The values have been depicted in Fig 8.

Table 2 : Incremental Permutation Passable for Triangle MIN

Fault	Total. Path Length	Total No. of requests matured	Average Path Length	% of requests Matured
No Fault	24	8	3	50
Mux	24	8	3	50
S1 n-cr S1 cr	32 16	8 4	4 4	50 25
S2 n-cr S2 cr	28 20	7 5	4 4	43 31
S3 n-cr S3 cr	28 24	7 6	4 4	43 37
S4	24	8	3	50
DEMUX	24	8	3	50

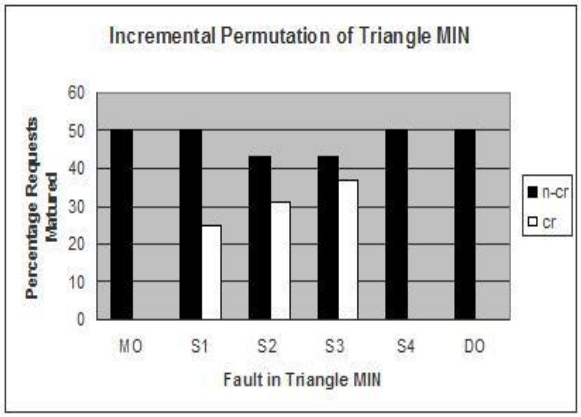

Fig 8

The table 3 shows the actual no of requests getting matured and their average path lengths for Quad Tree (QT) MIN.The values have been depicted in Fig 9.

Table 3 : Incremental Permutations Passable for QT

Fault	**Total Path Length**	**Total No. of requests matured**	**Average Path Length**	**% of requests Matured**
No Fault	20	4	5	25
Mux	20	4	5	25
S1 n-cr	20	4	5	25

S1 cr	20	4	5	25
S2 n-cr	15	3	5	18
S2 cr	10	2	5	12
S3 n-cr	10	2	5	12
S3 cr	0	0	0	0
S4 n-cr	15	3	5	18
S4 cr	10	2	5	12
S5	20	4	5	25
DEMUX	20	4	5	25

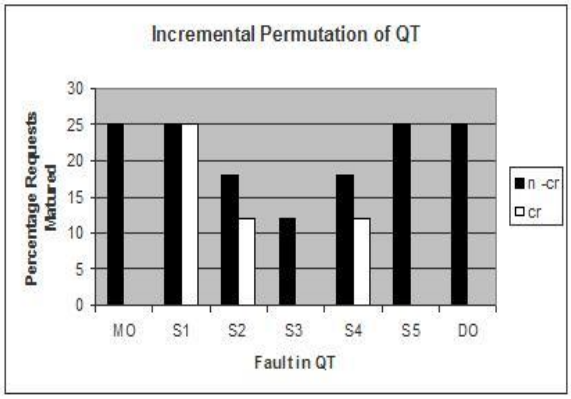

Fig 9

The table 4 shows the actual no of requests getting matured and their average path lengths for Phi (PHN) MIN.The values have been depicted in Fig 10.

The table 5 shows the actual no of requests getting matured and their average path lengths for Theta(THN) MIN.The values have been depicted in Fig 11.

Table 4 : Incremental Permutation Passable for PHN

Fault	Total Path Length	Total No. of request passes	Average Path Length	% passable of requests
No fault	16	4	4	25
Mux	16	4	4	25
S1 n-cr	16	4	4	25
S1 cr	12	3	4	18
S2 n-cr	16	4	4	25
S2 cr	12	3	4	18
S3 n-cr	16	4	4	25
S3 cr	12	3	4	18
S4	16	4	4	25
DEMUX	16	4	4	25

Table 5 : Incremental Permutation Passable for THN

Fault	Total Path Length	Total No. of requests matured	Average Path Length	% of requests matured
No Fault	32	8	4	50
Mux	32	8	4	50
S1 n-cr	24	6	4	37
S1 cr	16	4	4	25
S2 n-cr	24	6	4	37
S2 cr	16	4	4	25
S3 n-cr	24	6	4	37
S3 cr	16	4	4	25
S4	32	8	4	50
DEMUX	32	8	4	50

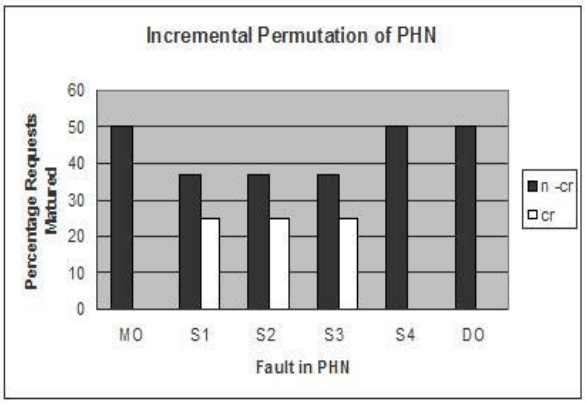

Fig 10

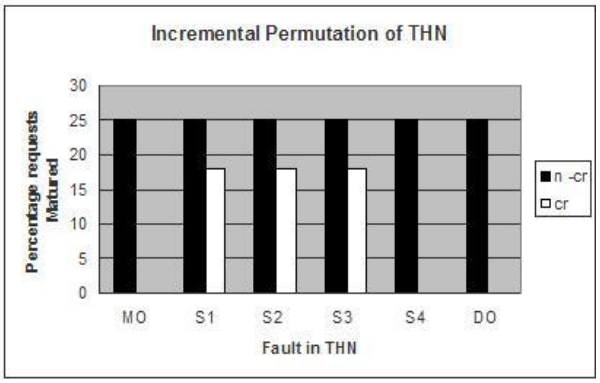

Fig 11

Method

A simulator in c# in .Net platform has been designed. All the performance parameters discussed have been analyzed on this simulator.

VIII. CONCLUSION

The proposed Fault Tolerant Irregular Triangle MIN is better as compared to the other discussed Networks. It has more bandwidth, probability of acceptance, processor utilization, processor power and throughput than popular MINs Omega, Quad tree, Theta and Phi Networks.

The proposed network has reduced latency as compared to 5 stages Quad Tree Network .The Triangle MIN has same no of stages as of Theta and Phi but has more no of requests getting matured in fault free as well as non critical and critical faulty components.

At the same time the proposed network has variable shorter path lengths from source to destination as compared to other discussed networks.

The Triangle Network has lesser no of Switching Elements (SEs) as compared to all the discussed Networks. It has 22 SEs as compared to 32 in Omega,

24 in Theta as well as in Phi and 26 in Quad Tree Network.

The average path length is significantly better in proposed Triangle Network.

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