Implementation of Voltage controlled Multi Device Interleaved Boost converter using FPGA

Divya Navamani.J, Lavanya.A, Vijayakumar.K

SRM University, Tamil Nadu, India
Email: divyateddy1@gmail.com, lavanya.a@ktr.srmuniv.ac.in, vijayakumar.k@ktr.srmuniv.ac.in

Abstract : In this paper, Multi device interleaved boost converter is studied and modeled. This converter has a high conversion ratio and achieves higher efficiency with reduced voltage and current stresses on the power semiconductor switches when compared with the conventional boost converter. Open loop and closed loop simulation with PI controller is done using MATLAB/SIMULINK and the results are compared. Hardware is done in the open loop and closed loop system using an FPGA with PI controller. Efficiency is obtained for different duty cycle and input voltage and compared to simulated results. A multi device structure with interleaved control is proposed to reduce the output voltage ripples with high efficiency for lesser duty cycle compared to other topologies. Experimental results are obtained for 20W, 40V prototype. The pulses are given through Spartan 6 FPGA which is programmed in VHDL coding. Simulation results are validated with hardware results.

Index Terms— MDIBC, Modelling, Voltage mode control, PI controller, Efficiency, FPGA

I. INTRODUCTION

Transportation is one of the major causes of air pollution. Electric Vehicle (EV) has recently emerged as viable alternative that uses pollution free battery power to produce clean energy to power the Vehicle. However, this new situation and tremendous increase in growth of EV can create serious problems of power quality in existing grids, mainly in the parking installation area [1, 2]. Thus, growing presence of EV battery chargers in residential installation could increase the harmonic level in power distribution systems and which in turn causes to reduce the distribution transformer life [3].High gain step up DC-DC converters have gained popularity in power Electronics applications including Electric, plug in ,hybrid and fuel cell vehicles.

Field Programmable Gate Array (FPGA) technology has developed rapidly over the last few years. The reconfigurable nature along with their high speed and flexibility has contributed greatly to their widespread use in a large number of control and signal processing applications. Added to this is the ability to incorporate multiple soft-core microcontrollers along with combinational and sequential logic modules on a single FPGA chip even on one with modest number of gates. The major challenges in high step-up DC/DC converters are the following

- How to extend the voltage gain and avoid the extreme duty cycle to reduce the current ripple and the conduction losses.
- How to reduce the switch voltage to make low voltage MOSFETs available. How to realize soft switching performance to reduce the switching losses.
- How to alleviate the output diode reverse-recovery problem, How to increase the power level easily and reduce the passive component size.

These constrains are taken and they were analyzed to choose the best converter for fuel cell without galvanic isolation [4-6]. Especially designing a converter with low ripple in the input side is necessary for the fuel cell application system. Hence this project is mainly based on the ripple analysis, stress analysis and efficiency analysis of input current of different converter used for the fuel cell application system

This paper is organized as follows. The mathematical modeling of MDIBC including the transfer function (control to output voltage) is reviewed in Section 2.Modeling of MDIBC with PI controller is presented in Section3. Hardware results are compared with simulation results in Section 4. Some conclusions are given in Section 5.

II. MATHEMATICAL MODEL OF MDIBC

The converter acts as a time-invariant system while the transistor is on. While the transistor is off, the converter acts as another time-invariant system and if the inductor current reaches zero, the converter acts as yet another time-invariant system. If the transistor is controlled as described previously, the converter can be described as switching between different time-invariant systems during the switching period. Consequently, the converter can be modeled as a time-variant system. State-space averaging is one method to approximate this time-variant system with a linear continuous-time time-invariant system. This

method uses the state space description of each time-invariant system as a starting point.

MDIBC has the highest gain ratio compared to all the other converters compared. But the duty cycle variation for this converter is applicable only till 0.49. Above that no output will be obtained. Even though the duty cycle is restricted to a very low value, high output is obtained than other converters. The modeling of MDIBC is done using state space averaging.

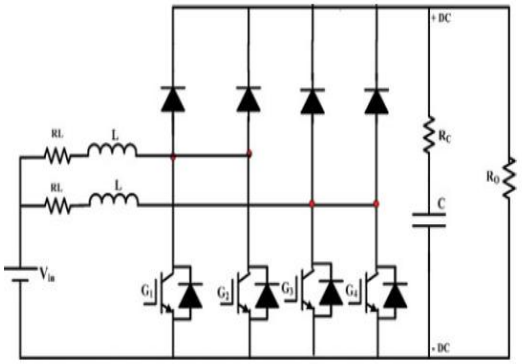


Fig.1 MDIBC converter

The state space variables are chosen and they are,

I_L – inductor current

V (t) – capacitor voltage

The general form of state space equation is,

$$\frac{dx(t)}{dt} = A1x(t) + B1u(t) \quad (1)$$

$$y(t) = C1x(t) + E1u(t) \quad (2)$$

$$\frac{d}{dt}\begin{bmatrix} IL \\ V(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \left[-\frac{1}{(R+Rc)c}\right] \end{bmatrix}\begin{bmatrix} IL \\ V(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} Vg \quad (3)$$

$$Y = [0 \quad \left[\frac{1}{(R+Rc)}\right]]\begin{bmatrix} IL \\ V(t) \end{bmatrix} \quad (4)$$

$$A = \begin{bmatrix} -\frac{RRc(1-D)}{(R+Rc)L} & -\frac{R(1-D)}{(R+Rc)L} \\ \frac{R(1-D)}{(R+Rc)} & \left[-\frac{1}{(R+Rc)C}\right] \end{bmatrix} \quad (5)$$

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (6)$$

$$C = [\frac{RRc(1-D)}{(R+Rc)} \quad \frac{R}{(R+Rc)}] \quad (7)$$

$$Ax + BU = 0 \quad (8)$$

$$Cx + EU = Y \quad (9)$$

$$0 = \frac{RRc(1-D)}{(R+Rc)} IL - \frac{R(1-D)}{(R+Rc)L} Vc + \frac{Vg}{L} \quad (10)$$

$$0 = \frac{R(1-D)IL}{(R+Rc)C} - \frac{1}{(R+Rc)C} Vc \quad (11)$$

$$\frac{Vo}{Vg} = \frac{1}{1-\frac{R}{(R+Rc)}D} \quad (12)$$

$$B = [B \quad Bd] \quad (13)$$

$$E = [E \quad Ed] \quad (14)$$

$$Bd = (A1 - A2)x + (B1 - B2)U \quad (15)$$

$$Ed = (C1 - C2)x + (E1 - E2)U \quad (16)$$

$$Bd = \begin{bmatrix} \frac{RRcIL}{(R+Rc)L} & \frac{RV}{(R+Rc)L} \\ \frac{-RIL}{(R+Rc)C} & 0 \end{bmatrix} x \quad (17)$$

$$Ed = \frac{-RRcILD}{(R+Rc)} \quad (18)$$

$$B = \begin{bmatrix} \frac{D}{L} & \frac{Vg}{L(1-D)} \\ 0 & \frac{-VgD}{(R(1-D)+Rc)C(1-D)} \end{bmatrix} \quad (19)$$

$$E = [0 \quad \frac{-RcVgD}{(R(1-D)+Rc)(1-D)}] \quad (20)$$

$$X(s) = (SI - A)^{-1} BU(S) \quad (21)$$

$$Y(s) = CX(S) + EU(S) \quad (22)$$

$$\frac{\frac{Vo(s)}{d(s)}}{} = \frac{Vg}{(1-D)^2} \frac{(1+SRcC)[(((1-D)^2Ro) - R_L) - SL]}{S^2LC(Ro+Rc) + S[L + CR_L(Ro+Rc) + ((1-D)^2RoRc)] + (R_L + (1-D)^2Ro} \quad (23)$$

After substituting the values for Duty cycle, R, L and C the control to output voltage transfer function

$$= -\frac{0.8[S^2 - 10013012.41S - 3.005 \times 10^{10}]}{[S^2 + 6.1245 \times 10^4 + 1.9463 \times 10^8]} \quad (3)$$

This gives the transfer function of multi device interleaved boost converter. Bode plot is drawn with this

transfer function by assuming the values of inductance and capacitance. Thus the open loop system can be analyzed and the stability of the system could be found. Equation (23) gives the derived transfer function of control to output voltage.

Figure 2 shows the graph of voltage gain versus duty cycle. Phase margin obtained from the bode plot is very low as shown in figure 3 and the pole zero plot shows that the zero lies in the RHP plane(figure 4) tells that the converter is not stable.

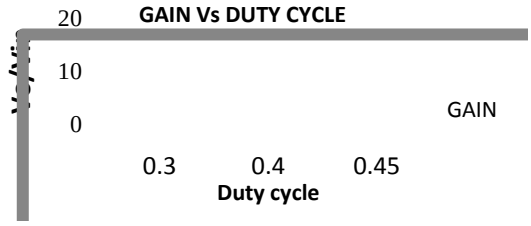


Fig 2. Voltage gain Vs duty cycle

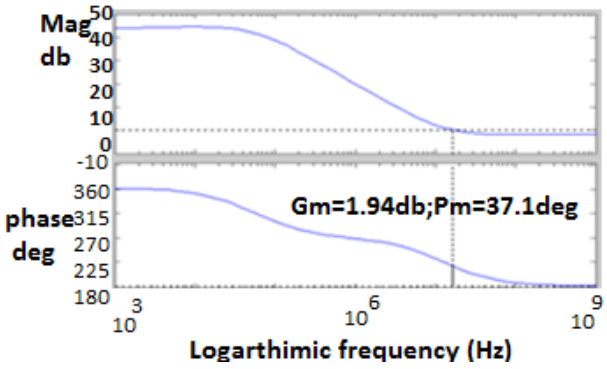


Fig 3, Bode plot of control to output voltage transfer function with gain and phase margin

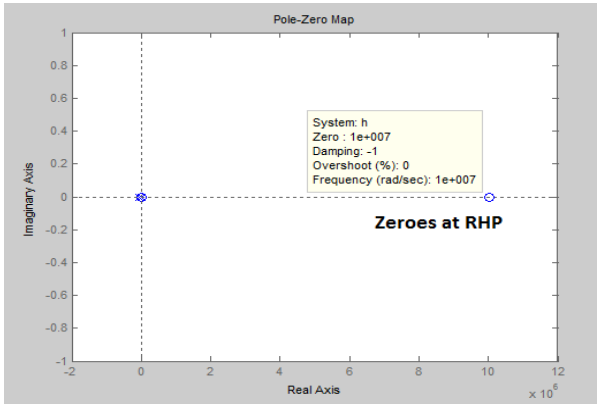


Fig 4. Pole zero map of transfer function

III. MODELING OF MDIBC WITH PI CONTROLLER

The general equations are written for the MDIBC converter. The equations are used to model the converter. The input voltage and duty cycle are given as inputs in the modelling without PI controller. With PI controller, the reference voltage is set as input.

$$V_o = V_c \tag{24}$$

$$V_c = \frac{1}{C}\int I_c\,dt \tag{25}$$

$$I_c = \frac{I_{L2}D}{2} - \frac{V_o D}{R} \tag{26}$$

$$L_2\frac{dI_{L2}}{dt} = \{V_g - r_{L2}I_{L2}\}D - \frac{V_c D}{2} \tag{27}$$

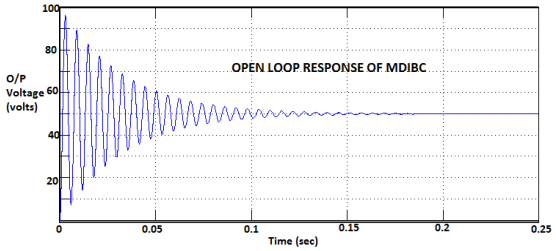


Fig 5. Open loop response of MDIBC

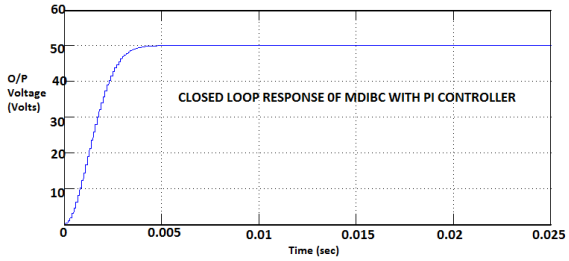


Fig 6. Closed loop response of MDIBC

Figure 5 and 6 shows that the open loop and closed loop response of MDIBC converter. It is clear that the converter reaches a steady state much earlier with PI controller than without PI controller

IV. HARDWARE IMPLEMENTATION

TABLE 1
TWO PHASE MDIBC SPECIFICATION

Device	Specification
Power MOSFET	IRF460-500V, 50A
Power diodes	ByQ28E-200E, 200V, 10A
Inductor	210uH
Capacitor	330uF
FPGA	Spartan-6

Table 1 shows the device specification. In order to improve the efficiency and to reduce the output voltage ripples of the converter, closed loop implementation of MDIBC is done using FPGA and PI Controller. The combination of proportional and integral terms is important to increase the speed of the response and also to eliminate the steady state error. The PID controller block is reduced to P and I blocks only. Proportional + Integral (PI) controllers were developed because of the desirable property that systems with open loop transfer functions of

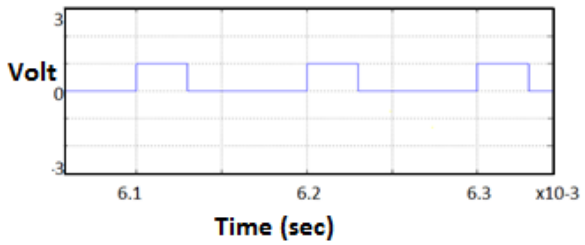
type 1 or above have zero steady state error with respect to a step input.

Tuning PI Controllers- General approach to tuning:

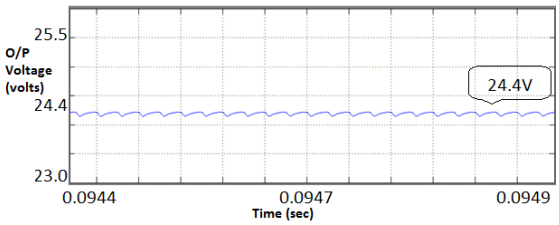
1. Initially have no integral gain (TI large)

2. Increase KP until get satisfactory response

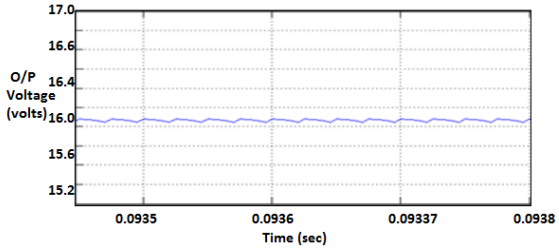
3. Start to add in integral (decreasing TI) until the steady state error is removed in satisfactory time.



(a)



(b)



(c)

Fig. 7. Simulated results (a) Pulse output(D=30%) (b)output voltage(d=30%) (c) Output voltage (d=20%)

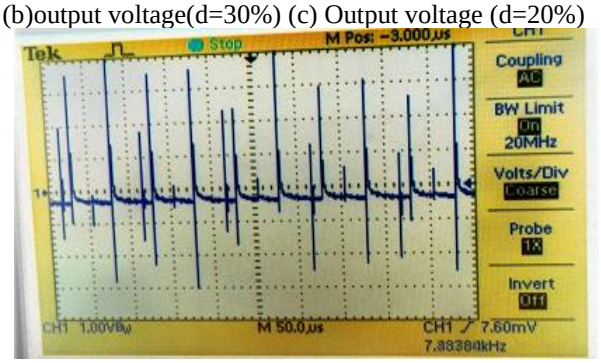
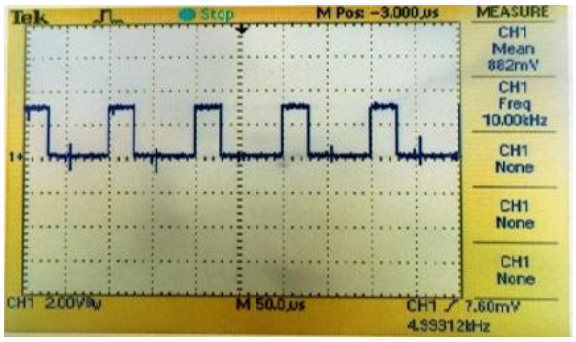
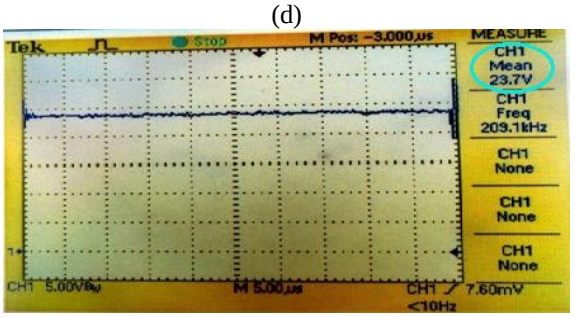


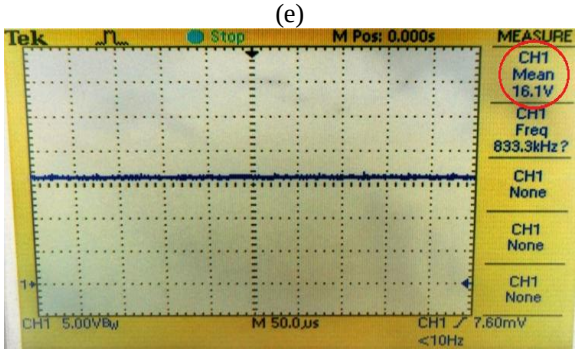
Fig. 8. Measured Output voltage ripples –Open loop



(d)



(e)



(f)

Fig. 9 Experimental results. (a) Pulse ouput(D=30%) (b)output voltage(d=30%) (c) Output voltage (d=20%)

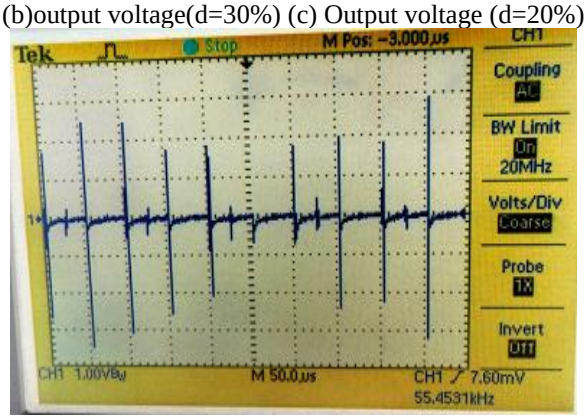


Fig.10. Measured output voltage ripples-Closed loop

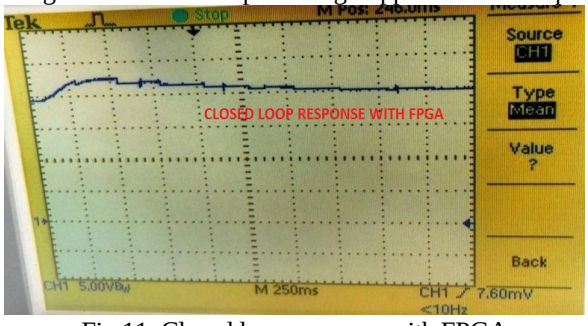


Fig.11. Closed loop response with FPGA

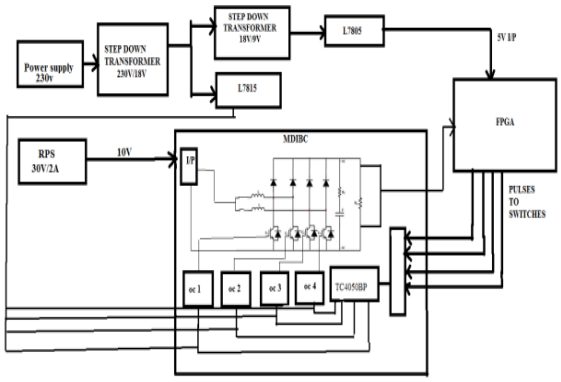
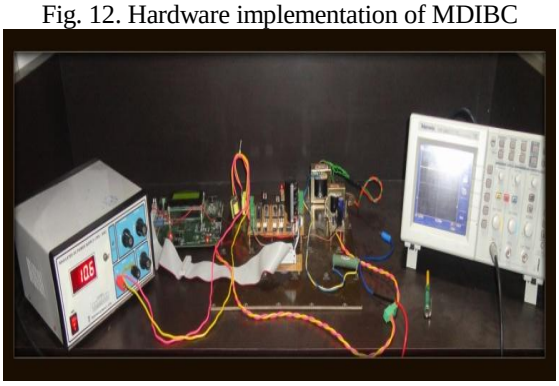
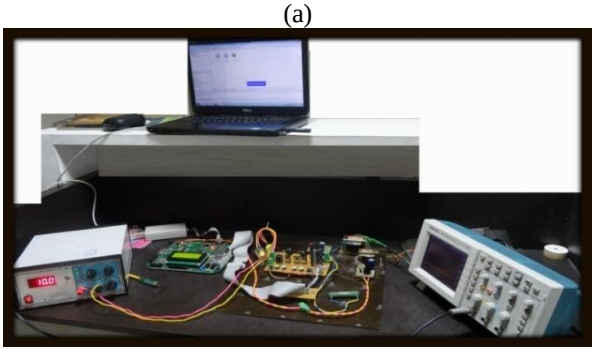


Fig. 12. Hardware implementation of MDIBC



(a)



(b)

Fig.13. Experimental setup. (a) Open loop (b) Closed loop

Complete experimental setup for open loop and closed loop system is shown in figure 13. Figure 7 and 9 shows the pulse output and output voltage obtained from simulation and hardware system. Hardware results are validated from the simulation results.Spartan-6 FPGA is used to obtain the pulses for both open loop and closed loop system.

Spartan-6 FPGA delivers an optimal balance of low risk, low cost, and low power for cost-sensitive applications, now with 42% less power consumption and 12% increased performance over previous generation devices. Spartan-6 FPGAs offer advanced power management technology, up to 150K logic cells, integrated PCI Express® blocks, advanced memory support, 250MHz DSP slices, and 3.2Gbps low-power transceivers. The Spartan-6 FPGA family comprises of two domain-optimized sub-families with a mix of features matched to stringent market requirements for price-sensitive, high-volume applications [7, 8]. Figure 12 shows the hardware implementation of MDIBC with PI controller and FPGA .The results obtained in the closed loop system as shown in figure 11 is validated with the results obtained from simulation of MDIBC as shown in figure 6.

The ripples in the Input current of DC-DC converter can be reduced by

(i) Increasing Switching frequency.

(ii) Increase Inductance value

The First condition increases the losses in the converter (Switching loss) which in turn reduces the efficiency of the converter. The second condition increases the weight and volume of the converter. Easy way to reduce the size of the inductor and capacitor is by increasing the frequency of the inductor current ripple and the output voltage ripple. Figure 8 and 10 shows the measured output voltage ripples obtained from the prototype. It is clear that the ripples obtained in the closed loop as shown in figure10 is reduced to greater amount as compared to the ripple output obtained in the open loop system. Figure 14 and 15 gives the efficiency curve of MDIBC for both open loop and closed loop system.

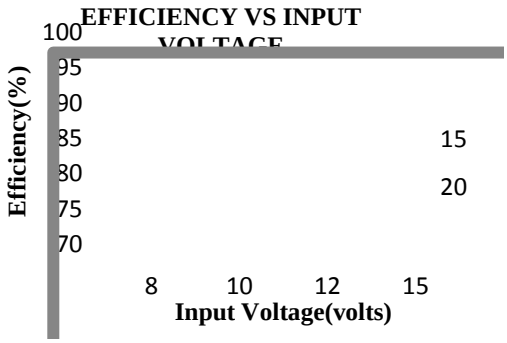


Fig 14. Efficiency Vs input voltage of MDIBC –Open loop

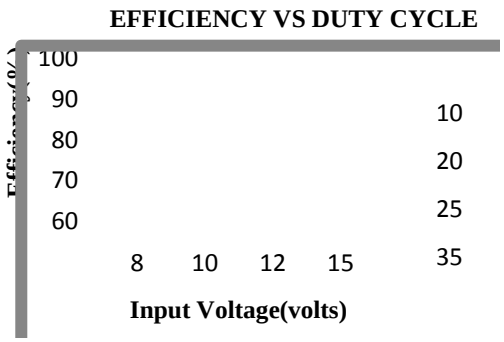


Fig 15. Efficiency vs duty cycle of MDIBC –closed loop

V. CONCLUSION

An Interleaved multi device boost converter operates efficiently with reduced voltage stress. The main drawback related to this topology output voltage ripple. In

order to reduce the ripple, a thorough study on MDIBC was made and modeling of the converter was also done. Simulation was done for both open loop of MDIBC and closed loop modeling of MDIBC with PI controller. Hard ware prototype was created for both open loop and closed loop with FPGA and PI controller. The ripple content in the closed is found to be much lesser in the open loop. Also using PI controller, the output attains a steady state much faster.

REFERENCES

[1] Valsera-Naranjo, E. and Sumper, A. and Lloret-Gallego, P. and Villafafila-Robles, R. and Sudria-Andreu, .,"Electrical vehicles: State of art and issues for their connection to the network", 10th International Conf. on Electrical Power Quality and Utilisation, 2009. EPQU 2009.,pp. 1-3, Sept. 2009.

[2] Putrus, G.A. and Suwanapingkarl, P. and Johnston, D. and Bentley, E.C.and Narayana, M.,"Impact of electric vehicles on power distribution networks", IEEE Vehicle Power and Propulsion Conference, 2009. VPPC '09., pp. 827-831, Sep. 2009.

[3] Gomez, J.C. and Morcos, M.M."Impact of EV battery chargers on the power quality of distribution systems",IEEE Trans.on Power Delivery,vol. 18,no. 3, pp. 975-981, Oct. 2003.

[4] D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," IEEE Trans. Power Electron., vol.3, no.4, pp. 484-488, Oct. 1988.

[5] R. J. Wai, R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," in Proc. IEE-Elect. Power Applicat., vol. 152, no. 4, pp. 793–802, Jul. 2005.

[6] R. J. Wai, R. Y. Duan, "High-efficiency power conversion for low power fuel cell generation system," IEEE Trans. Power Electron., vol. 20, no.4, pp. 847-856, Jul. 2005.

[7] http://www.inipro.net- Xilinx FPGA

[8] http://www.directindustry.com/prod/xilinx/ field-programmable-gate-arrays - Xilinx FPGA

◈◈◈