Advance Physics Letter

Analysis and Simulation of a Cascaded H-Bridge Structure Electrical Converter With Separate DC Supply

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Abstract--- The construction thought is employed to decrease the harmonic distortion within the output wave shape while not decreasing the electrical converter power output. construction inverters with an outsized range of steps will generate prime quality voltage waveforms, adequate to be thought of as appropriate voltage supply generators. A changed curving Pulse dimension Modulation (SPWM) modulator with section disposition that will increase output wave shape up to 7-level whereas reducing output harmonics is conferred during this paper. The output wave shape of asymmetrical topology is inflated up to 7- level by exploitation twin separate DC sources (SDCSs). The DC provide demand of asymmetrical cascaded topology is solved exploitation twin sources rather than six SDCSs.

Keywords— Harmonic suppression, Multilevel Inverter, Total Harmonic Distortion.

I. INTRODUCTION

The construction inverters (MLI) are performed exploitation 3 level inverters projected by Nabae. within the study, the third level has been established by exploitation neutral purpose of DC line and also the topology has been outlined as Diode Clamped (DC-MLI) [1]-[2]. In recent years, MLIs have gained abundant attention within the application areas of medium voltage and high power thanks to their numerous blessings like lower common mode voltage.

The most common MLI topologies classified into three types are Diode Clamped MLI (DC-MLI), Flying Capacitor MLI (FC-MLI), and Cascaded H-Bridge MLI (CHB-MLI).The Hybrid and Asymmetric Hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively [7], [10]. The cascaded multilevel topology that contains dual H-bridge has been shown in Fig.1.

Each single phase H-bridge generates three voltage levels as +Vdc, 0, -Vdc connecting the DC source to the AC output by different combinations of four switches, SA1, SA1 1, SA2, and SA2 1 as seen in first cell of Fig. 1. The CHB-MLI depicted in Fig.1 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain +Vdc, SA1 and SA2 1 switches are turned on, whereas -Vdc level can be obtained by turning on the SA2 and SA1 1. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as seen in (1). The switching states of a CHBMLI can be determined using (2) [11].

$$m = 2n+1 \quad (1)$$

$$sw = 3m \quad (2)$$

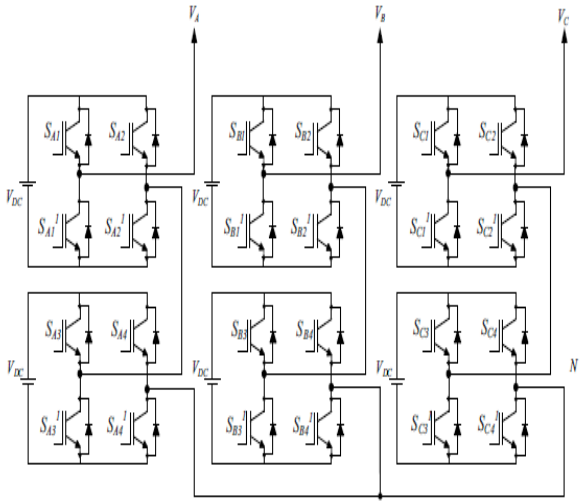

Fig. 1. Three phase five-level topology of cascaded H-bridge multilevel inverter

The hybrid construction topologies ar entrenched victimisation combination of 2 basic topologies of DC-MLI and FCMLI. The topology utilizes DC-MLI or FC-MLI to exchange the H-bridge because the basic module of the CHB-MLI so as to scale back the amount of the separated DC sources. differing kinds of feed-forward and feed-back PWM management schemes are developed to regulate VSIs. SPWM technique is one among the foremost common modulations Techniques among the others applied in power switch inverters. In SPWM, a curved reference voltage wave shape is compared with a triangular carrier wave shape to get

gate signals for the switches of electrical converter. The carrier signal in SPWM modulation technique generally includes a frequency within the vary up to twenty kHz. The switch angle of multi-switching management signal (Ssw(t)) of the electrical converter is calculated by Fourier series to eliminate hand-picked harmonics as in (3)

$$S_{sw}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) \qquad (3)$$

where a0 is the average dc value of the switching signal.

II. ASYMMETRIC CASCADED TOPOLOGY OF MLI

A. Basic Principle of Multilevel Inverter and Design

Fig. 2 shows the most H-bridge cell of associate electrical converter used for implementation of the structure electrical converter. the total bridge electrical converter module includes four power switches and 4 clamping diodes to create associate H-bridge. A structure cascade electrical converter consists of variety of H-bridge cells that connected series per section, and every module need s a separate DC supply to get voltage levels at the output of electrical converter. The switch inputs shown as In1..4 within the Fig. two can enable getting output voltages of every H- bridge as follows;

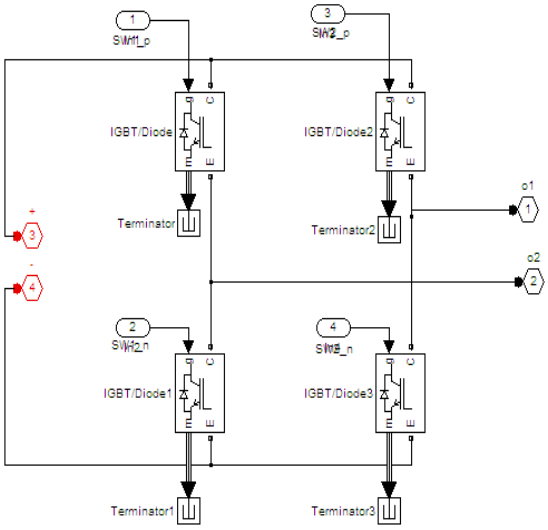

Fig. 2. Three-level full bridge module

The switching angles that are indicated as Θ1… Θ5 in (6) can be chosen to obtain minimum voltage harmonics. CHBMLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources.

Fig. 2 depicts one cell of the phase of Fig. 1. The first leg phase voltage (Van) of Fig. 1 is constituted by multiplying Va1 and Va2 values of series connected H-bridge cells and will generate a stepped waveform as seen in Fig. 3.

B. The Power Block of Designed Multilevel Inverter

The cascaded MLI has been established victimisation IGBT Hbridges that have 2Vdc supply at the upper side of phase legs and Vdc supply at the lower side. The whole style that contains switch devices and management block is delineate in Fig. 4. The cascaded MLI block is switched by the projected 24-channel SPWM modulator to get 7-level output at the back-end of the 3-phase voltage supply electrical converter. The SPWM modulator generates the management signals

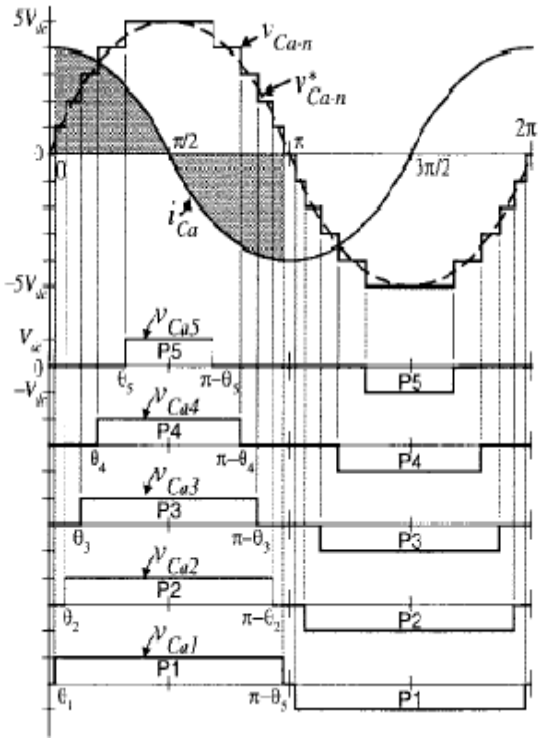

Fig. 3. Phase output voltage waveforms of a five-level topology CHB-MLI with 2 separate DC sources

according to phase disposition (PD) carrier signals to calculate the most accurate switching angles. The cascaded MLI inverter block is shown in Fig. 5. The H-bridge cells are constituted as seen in Fig. 2 using IGBTs and parallel diodes to achieve fast and reliable switching cells. All the phase legs has dual switching cells which are controlled using complementary switching orders to generate a staircase voltage waveform at the output.

The shift orders of Fig.2 has been utilised to point variety of devices as In1…4 for the higher H-bridge cell and In1_2…4_2 for the lower cell in an exceedingly section leg. The output voltage of cascaded electrical converter is obtained by adding the output voltage of every cell and therefore the way wave shape illustrates 7-level output

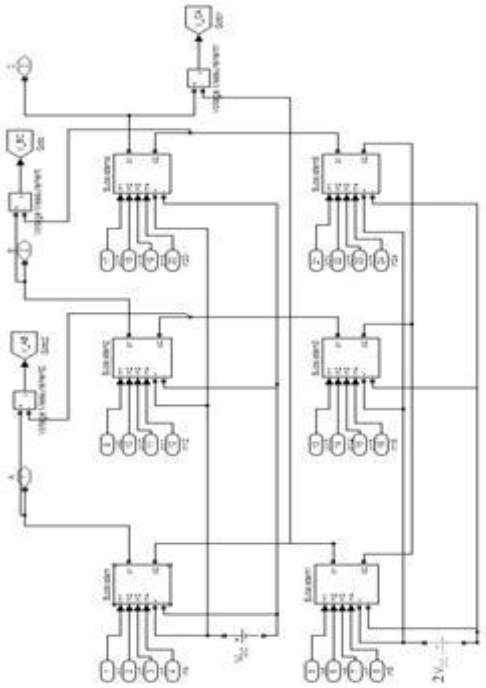

Fig.5. Block diagram of cascaded H-bridges with 2 separate DC sources

III. DESIGN OF MODULATOR BLOCK

The most well known SPWM which can be applied to cascaded multilevel inverters is phase shifted SPWM and is same as that of the conventional SPWM technique as seen in Fig. 3 of [2].

The vertical carrier distribution techniques are defined as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD), while horizontal arrangement is known as Phase Shifted (PS) control technique.

The control signal patterns which switch the inverter block to generate +Vdc and +2Vdc levels at the output of Phase A has been depicted in Fig. 6. Fig. 6 (a) shows triangular carrier signals and modulating signal. Control signal of the upper H bridge cell is generated according to comparing the first carrier and is shown in Fig. 6 (b) while the second carrier comparison result is illustrated in Fig. 6 (c).

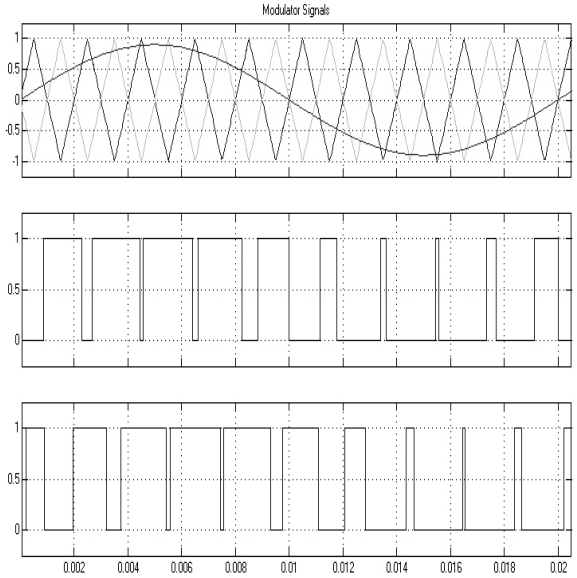

Fig. 6. Modulator signals (a) phase disposition carrier signals and modulating signal (b) SPWM output of 1st carrier (c) SPWM output of 2nd carrier

Fig. 7 shows the control signals of a phase generated by the phase disposition and modulator block in Matlab/Simulink. 1st and 3rd control signals are obtained according to initial carrier signal and 2nd and 4th signals are generated by comparing 2nd carrier with the modulating sinusoidal signal. The other four switching signals are achieved as negative complements of the first part of control signals. Fig. 8 shows the line-to-line voltage output of cascaded MLI with PD-SPWM control algorithm. The output patterns are obtained using modulation index (mi) value of 0.8 and the switching frequency (fsw) is 2.5khz

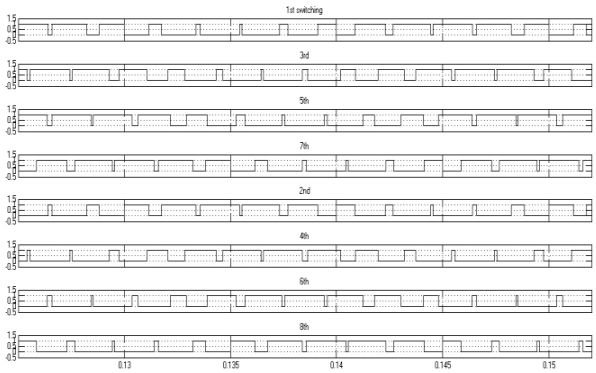

Fig. 7. Generated PD-SPWM switching signals for Phase A

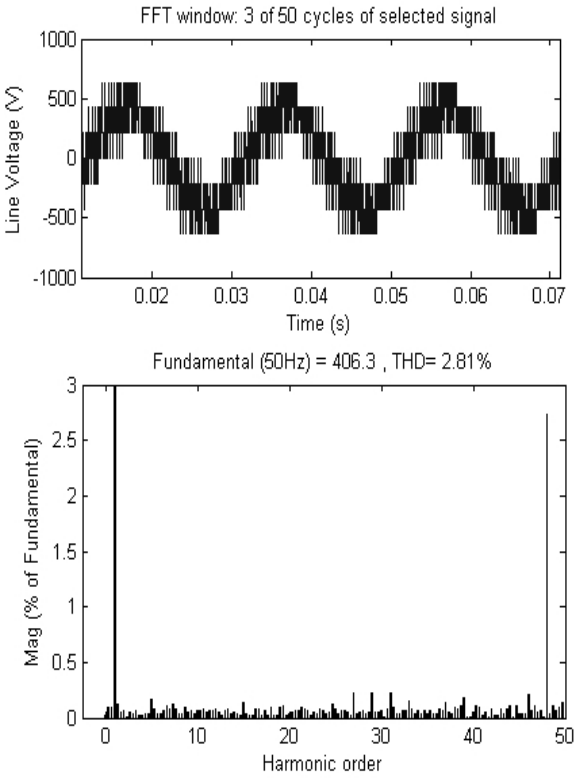

Fig. 8. 7-level line-to-line output voltage of inverter obtained at 2.5 kHz switching frequency

IV. HARMONIC ANALYSIS AND SIMULATION PROCESS

The SPWM modulator features a switch information measure between 0- twenty kHz to manage H-bridges and Fig. nine shows the values that area unit obtained at five kHz switch conditions whereas mi= zero.8. Fig. 9(a) and Fig. 9(b) represent the FFT analysis of the present doctor's degree (THDi) and voltage doctor's degree (THDv) ratios in Simulink. very cheap doctor's degree for current has been measured as zero.00% throughout five kHz switch frequency and mi= zero.8 conditions. The switch frequency of SPWM modulator has been restricted to 1-10 kHz, and modulation indexes area unit elect in zero.6≤ mi≤ 1.4 ranges to research the result of fsw and mi on doctor's degree of electrical converter.

It has been observed by the performed tests that reducing the THD of current and voltage is depended on increasing the switching frequency in linear modulation range up to 5 kHz. The output voltage waveform has been distorted when the modulation ratio exceed 100 around 5 kHz as compared in Fig. 10 (a) and Fig. 10 (b).

V. CONCLUSIONS

In this paper, a three-phase 7-level cascaded construction electrical converter with part disposition SPWM management has been conferred, achieving output signals with prime quality and really low doctorate thanks to robustly designed mathematical model of multi-carrier modulator. The spectral errors, like shift fall and rise times and therefore the amplitude distortions of the SPWM waveforms that cause distortions at output signals are reduced by victimisation multi-carrier SPWM in line with previous studies and literature. The shift actions are sculptural in Simulink by victimisation interpolation processes to get properly queued modulation signals.

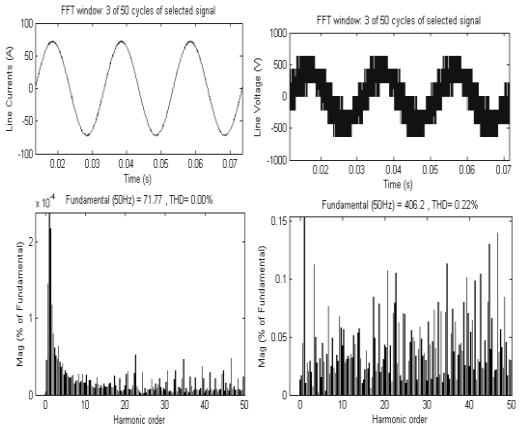

Fig. 9. THD analysis of inverter while fsw= 5 kHz and mi=0.8 (a) THD for current is 0.00% (b) THD for phase voltage is 0.22%

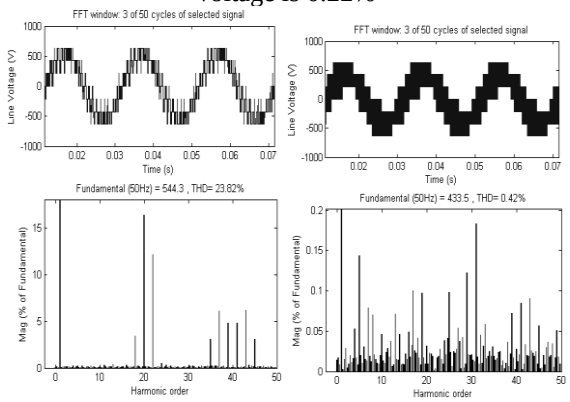

Fig. 10. THD voltage analysis while mi=1 (a) THD for voltage is 23.82% at 1 kHz switching (b) THD for voltage is 0.42 % at 10 kHz switching

The part shift and disposition orders of modulating signals ar another vital purpose of style to cut back ThD of line current and voltages. The change orders ar vital thanks to transferring change signals to semiconductors fitly and conjointly preventing DC bus short. The electrical converter block has been styleed exploitation twin H-bridges per part and also the MLI style has been equipped by twin SDCSs rather than half dozen provides to decrease value of experimental design. The measure results have given good outcomes on ThD analysis. The modulation indexes in over modulation vary have caused non linear changes in ThD values of output current and voltages.It is conjointly seen that the change frequency is directly effective on ThD. The increment in change frequency has showed its reducer result on ThD of output current and voltages. additionally, the measured harmonic contents have seen as basic (50 cycle per second, 1st), 46th, and forty eighth harmonics over two.5 kHz change conditions of linear modulation space (mi≤1). all-time low ThD of output voltage has

been measured as zero.22% in linear modulation band at five kHz change frequency. the foremost effective harmonic contents of output current have seen below zero.1% at forty sixth and forty eighth in analysis. The accuracy of style are verified with the results of continuous experimental studies.

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